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Military EMBEDDED SYSTEMS

VOLUME 4 NUMBER 2
MAR/APR 2008

INCLUDING:

MIL/COTS DIGEST SUPPLEMENT

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GPUs and scan conversion

OS trends:
Interoperable legacy code meets new platforms

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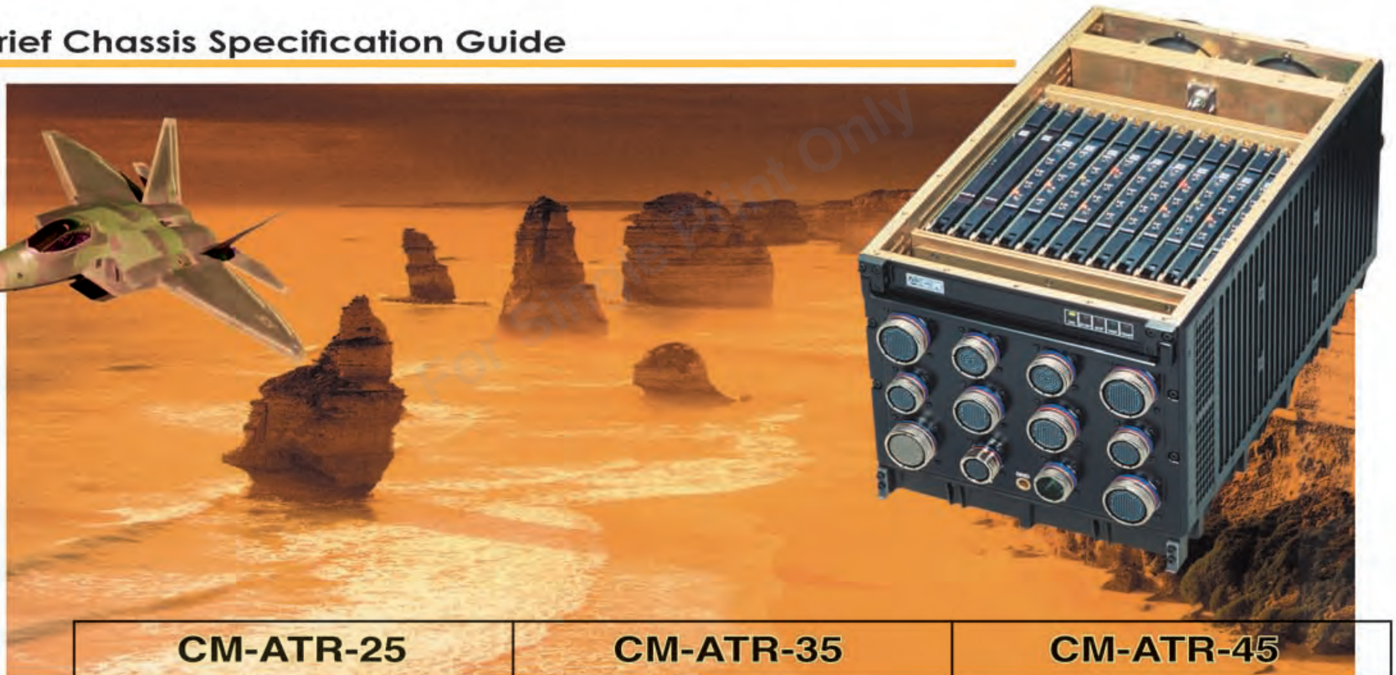

	CM-ATR-25					CM-ATR-35					CM-ATR-45				
(*)	*FAC*	*S*	*SEF*	*HES*	*SIXHEX*	*FAC*	*S*	*SEF*	*HES*	*SIXHEX*	*FAC*	*S*	*SEF*	*HES*	*SIXHEX*
Size / Slots	**½ ATR - Long / 5 Slot 6U VME64x or cPCI**					**¾ ATR - Long / 7 Slot 6U VME64x or cPCI**					**1 ATR - Long / 12 Slot 6U VME64x or cPCI**				
Power Supply	400 Watts				575 Watts	500 Watts				775 Watts	1050 Watts				1450 Watts
+5 / +3.3 VDC	20 Amp / 23 Amp				40 A / 23 A	40 Amp / 23 Amp				80 A / 23 A	80 Amp / 45 Amp				160 A / 45 A
±12 VDC	12 Amp each					12 Amp each					20 Amp each				
Chassis Vin	All PSU models accept: 28 VDC; 48 VDC; 270 VDC; Autorange 90-264 VAC @ 47-880 Hz and 200 VAC 3-Phase @ 47-880 Hz														
Board Format	Slot-by-slot user configured card-cage allows intermixing conduction-cooled IEEE-1101.2/ANSI-VITA 30.1 and air-cooled IEC-297/IEEE-1101.1 boards														

(*) Cooling Options: FAC - Flowthrough Air Cooled; **S** - Sealed; **SEF** - Sealed, Extended Fins; **HES** - Sealed, Heat Exchanger Sidewalls; **SIXHES** - Sealed, Six Heat Exchangers

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Military EMBEDDED SYSTEMS

March/April Volume 4 Number 2

COLUMNS

DEPARTMENTS

E-CASTS

www.mil-embedded.com/ecast

SDR is more than JTRS: Think military wireless networks and civilian mobile infrastructure
May 21, 2008 – 2 p.m. EDT
Sponsored by Red Rapids, PrismTech, Pentek, and Zeligsoft
Moderated by Chris A. Ciufo

ON THE COVER:
According to the GAO and DoD, the Army's Future Combat Systems (FCS) is America's largest military program *ever*. As reported in *The Washington Post*, the Army originally estimated 34 million lines of software in FCS. But due to changes in the scope of the development, the new projection is 63.8 million. It is an absolute certainty that not all of this code will be brand new, and that some of it will either be legacy modules from other programs or ATDs, or some will be required to interface with legacy systems. Either way: The importance of legacy software migration is critical. In our summary of "Military OS trends you'll want to know about," migration is just one of several messages revealed by our industry survey (article, page 16).

MQ-8B Navy Fire Scout picture courtesy of Northrop Grumman.

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CORRECTION: An Editor's Choice product in our Jan/Feb edition misidentified Curtiss-Wright's VPX6-684 Fireblade II as the VPX6-685 Fireblade II.

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Industry Analysis

The next great electronics program

By Don Dingee

There are hundreds of electronics technologies that shaped defense capability over the last century. Mobile two-way radio. Radar. Inertial guidance. Proximity fusing. Infrared seeker technology. Nuclear device triggering. Electronic jamming and countermeasures. Computer-based encryption. Fiber optics. Night vision. Fly-by-wire. Global positioning systems. Phased-array radar. Software-Defined Radio.

What will drive the next great electronics program? In the near term, information rules, and technologies to gather, manage, present, and secure it are high-value opportunities. In the longer term, a new wave of breakthroughs is needed for new types of systems.

Near term: Managing information

Programs such as the AEGIS Combat System and FBCB2 (Force XXI Battle Command Brigade and Below) are just the start in gathering, managing, and presenting information. Synthetic vision technology merges databases with information on terrain, obstacles, geo-political details, and other situational data with real-time information from GPS, video, and other sensors to create a total situational awareness solution. Digesting all this information into an easily understood and actionable 3D display (Figure 1, courtesy of Quantum3D) reduces information overload and makes manned vehicles more effective, while creating a high-fidelity experience for operating unmanned vehicles as well.

Protecting all this information is vital. Digital armor technology does what it suggests: It prevents hackers from accessing sophisticated electronics systems in armored vehicles and aircraft. Advanced firewalls including the MESHnet Firewall (Figure 2), jointly developed by General Dynamics Canada and Secure Computing, are being created to protect these connected assets. The MESHnet Firewall deploys Secure Computing's proven Sidewinder firewall in a rugged, conduction-cooled package ready for combat duty.

Longer term: Managing physics

Systems such as directed energy devices, electromagnetic rail guns or coil guns, and others call for advancements in electronics capability, survivability, and reliability to handle the sheer physics involved.

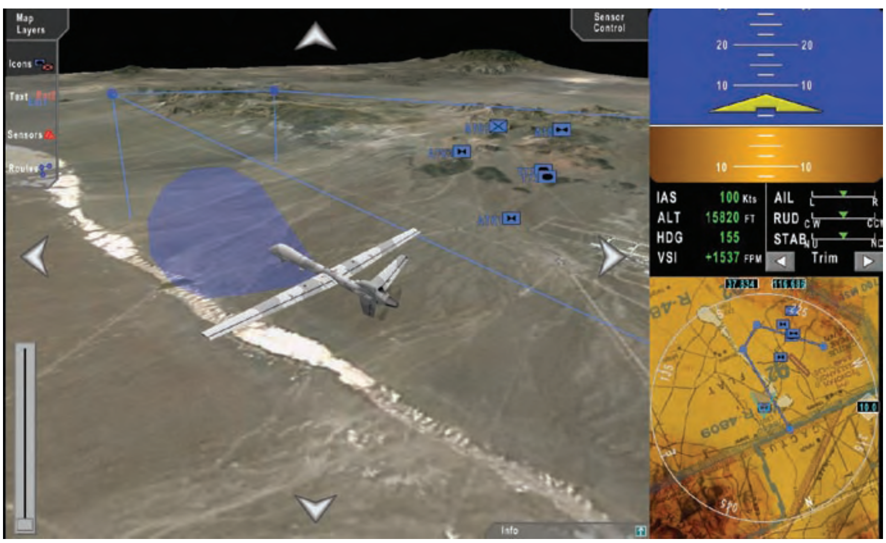


Figure 1

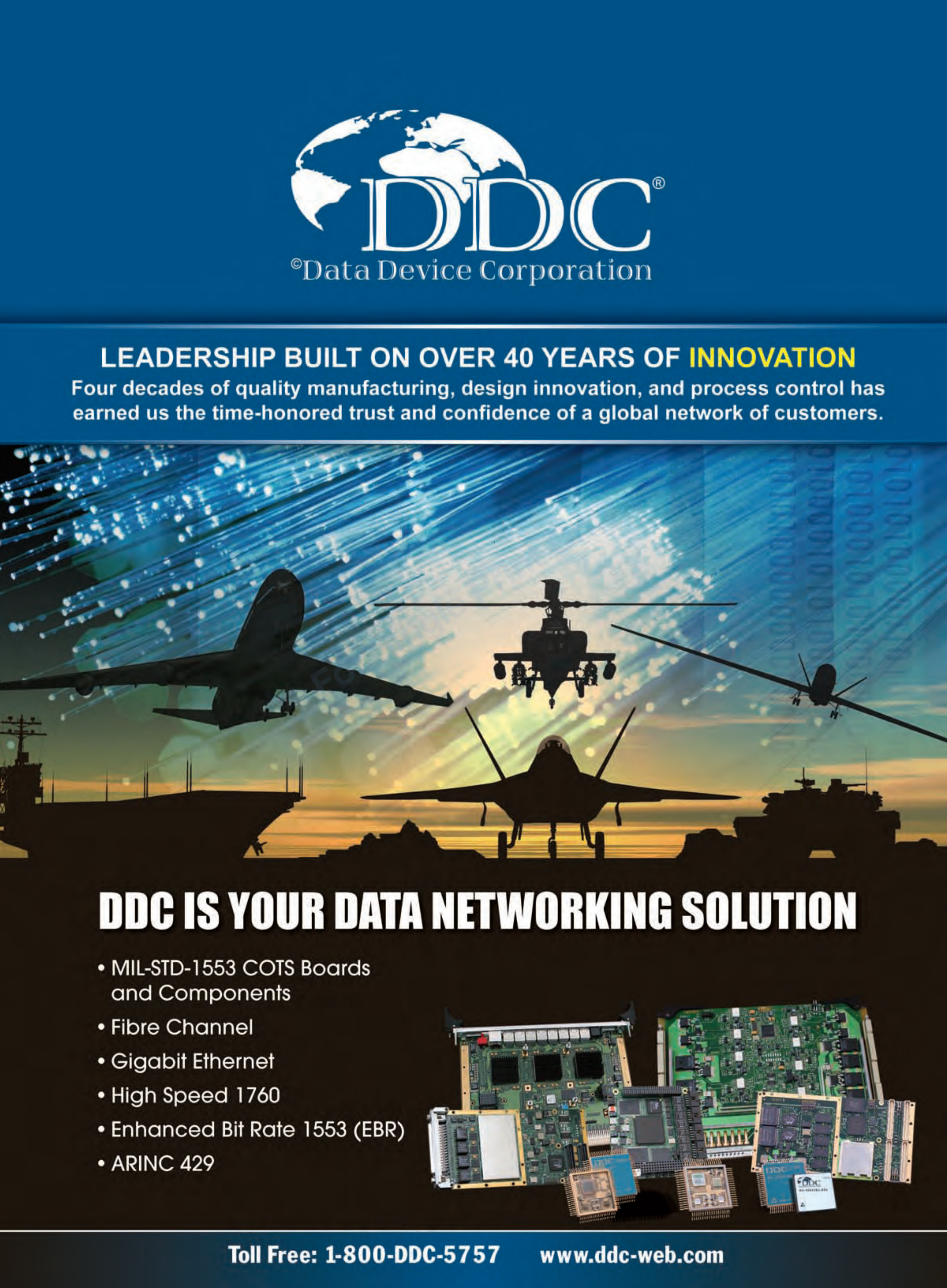
Figure 2

The Active Denial System uses a 95 GHz beam for crowd control, creating a sensation "too hot to bear without diving for cover" as a reporter and test subject from Reuters described after a 2007 demonstration. The vehicle-mounted beam penetrates skin about 1/64 of an inch, doing no damage but stimulating heat-sensing nerves, causing enough discomfort to cause crowds to disperse quickly.

Rail-gun technology envisioned for the U.S. Navy's DD(X) can theoretically launch a smart 3-foot long, 40-pound projectile up to 290 miles. But the forces involved are enormous, even in the initial 8 MJ versions. Generating 32 or 64 MJ requires big capacitive storage and arc-prevention technology. Surviving 45,000 *g* at launch requires rethinking the entire electronics payload design approach. On January 31, the brand new 32 MJ prototype was test fired for the first time at a 10 MJ level; we'll be watching as the tests continue.

Chances are good that when the next great defense electronics program emerges, it will contain new information and power electronics technology unimagined a decade ago, perhaps even turning science fiction into science fact.

For more information, contact Don at ddingee@opensystems-publishing.com.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Field Intelligence

Multicomputer software development systems come of age

By Duncan Young

It was not so long ago that the typical DSP development package was a set of optimized libraries, plus a port to the industry standard Vector Signal Image Processing Library (VSIPL) and a driver for an RTOS. While these are still essential elements for algorithm development, the platforms that host DSP applications have become much more complex, offering FPGA front ends and multicompute engines for DSP and general purpose processors for back-end interfacing to displays and data processing systems. The tools required to visualize, model, program, and debug these systems have also become more complex, supporting a wide variety of hardware architectures and configurations.

Visualization and modeling

Creating a complete, dynamic model of the system to be implemented, tested, and validated is a vital part of the design and development process. In the large majority of military DSP applications, it is unlikely that a single processor would have the capacity to resolve the problem alone. It needs to be broken down into smaller tasks, data flows, and processing capacity and then mapped onto available hardware capability. Thus, COTS vendors now offer the tools to describe and visualize this design process from the creation of a task structure to the hardware features of their products. These might include number and type of processors per module, memory capacity and bandwidth, interconnect type and bandwidth between processors, plus interconnects between modules using fabrics. By understanding the relationship between these features and the system's performance requirements, decisions can be made on how the application is constructed and distributed across multiple modules and processing nodes.

The same models translate into the test and verification of a real system. Tools are used to verify hardware configuration, to download and test selected parts of the application, and to analyze and debug the behavior of multiple processing nodes in real time. Accurately time-stamped data is collected by lightweight instrumentation to display data flows, processing times, and events – and to compare them with predicted values generated during the design process. Figure 1 illustrates a typical display of task, processor, and fabric activity captured by GE Fanuc Intelligent Platforms' AXIS integrated development environment, which supports the complete development cycle of these complex multicomputing systems.

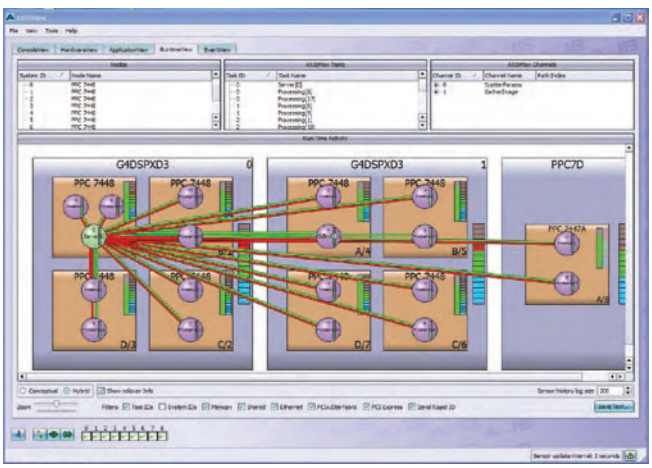

Figure 1

Communications

COTS vendors have created scalable multicomputing architectures to deal with the complexity of many military DSP applications. These require large numbers of compute nodes and high-bandwidth data paths to communicate between them. This complexity impacts the application developer in two ways. First, it requires a communications infrastructure to be developed between nodes and across fabrics. Second, it requires constant maintenance and support if hardware devices or fabric types were to change, which is natural as COTS hardware platforms evolve.

While current generations of hardware use PCI-similar fabrics such as StarFabric, new standards point to the widespread adoption of Serial RapidIO, PCIe, and 10 GbE for these multicomputer fabrics. To preempt these changes and make their products easier to use, COTS vendors are offering feature-rich interprocessor communications APIs that will remain constant, whatever the fabric's hardware implementation. This abstraction will also extend to RTOSs as the API grows to encompass the broader range of calls used to implement a DSP application, offering an almost transparent choice of RTOS, fabric, and processor to the user.

DSP libraries

Military applications generally use floating point math for accuracy and speed. Accordingly, the popular choice is Freescale Semiconductor's Power Architecture processor with AltiVec or specialized DSP processing devices such as Analog Devices' TigerSHARC. Power Architecture offers the advantage that processing nodes can also be used more easily for general purpose processing and management tasks to maintain a common hardware and development tool base across an entire system development. DSP function libraries for the respective processor types, often optimized by the module vendor, complete the development toolset, allowing the user to extract maximum performance from a specific hardware implementation.

While the DSP library is undoubtedly a vital element in DSP algorithm development, its impact on the overall development cost, timescales, and through-life sustainment costs of a complex new multicomputing development project is overshadowed by the broader toolsets now offered by hardware vendors. Modeling, visualization, verification, and abstraction tools are all good indications of the newfound maturity of the technology and its success in the future.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

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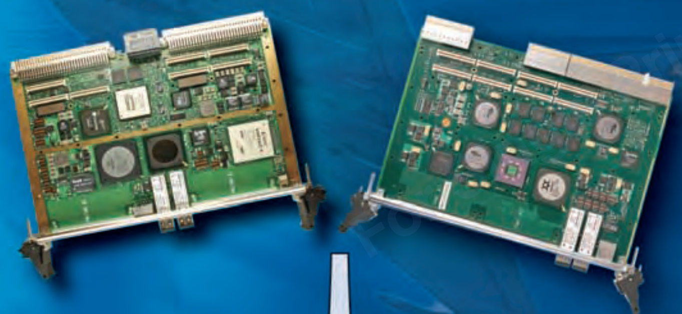

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Graphics Processing Unit accelerates scan conversion

By John Wemekamp

Many examples abound as to why the adoption of COTS technologies has been such a success story for the military. The maximum benefit is obtainable where massive commercial technology investment can be leveraged directly to solve a similar technology problem in another domain. Nowhere is this level of investment more evident than in the commercial video gaming market, providing the opportunity for the technology being developed for real-time, dynamic, and highly realistic gaming to be applied with an innovative twist to military applications. Examples of this include radar scan conversion or image processing on live sensor data streams.

The majority of surveillance radars still use rotating antennae, whether they are in fixed ground positions or mounted on ships or large aircraft. Once digitized, radar video output is in polar form (range and azimuth), which must be converted to raster format for display on an operator's screen. This scan conversion process is a very intense and repetitive algorithm that has traditionally been performed by a host processor or, more recently, with FPGA assistance to a host processor. The slow decay of data in the display buffer results in trails forming behind moving objects, making them clearly visible.

Off-the-shelf embedded computers are used extensively for the display and processing elements of radar systems. These computers can range from embeddable, industrial PCs for benign environment applications to VMEbus or its newer sibling VPX for harsher, more critical environments. Using current technology, the embedded host computer in the form of an SBC would be supported by a scan converter for displaying and windowing the radar image, plus a separate GPU to overlay graphics onto the radar and present a broader operational picture to the operator. These functions are typically implemented as PCI or PMC modules attached to the host SBC.

The demands of increasingly sophisticated, and hence more expensive to produce, video games are driving the investment in GPUs and the tools to support them. These GPUs are part of continuously evolving families of products necessarily offering application portability across generations and manufacturers. In the search for greater performance, the latest offerings from vendors such as NVIDIA and ATI incorporate large memory space and very high-performance, general-purpose processing capability. These support single-thread processes used in fragment and vertex manipulation required by real-time, three-dimensional (3D) animation. This on-GPU processing allows much faster image rendering directly into display memory than would be possible using a host processor. Until recently, it was difficult to make use of this latent capability; however, the introduction of shader languages – such as OpenGL's Shader Language (GLSL) or the High Level Shader Language (HLSL) supported by Microsoft – makes for much simpler programming of these functions using C code.

By loading the incoming radar in polar form into GPU memory, an algorithm running on the GPU can directly convert it into raster format in display memory in real time. Used in this way, the latest generations of GPUs offer an order of magnitude improvement in performance over FPGA-assisted scan converter solutions. For example, it is normally anticipated that an increase in display resolution will impact scan converter performance as more pixel locations are manipulated. However, Cohen using the GPU even with display resolutions of 2k x 2k pixels – often used for air traffic control or naval surveillance radars – there is no impact on overall performance. Additionally, displaying the traditional plan view of the radar image, the GPU allows the image to be easily distorted in real time to show projections from different origins and angles. This is illustrated in Figure 1, which shows a high-resolution, scan-converted and projected radar image created by the patent-pending SoftScan developed by Curtiss-Wright Controls Embedded Computing (CWCEC) using GLSL.

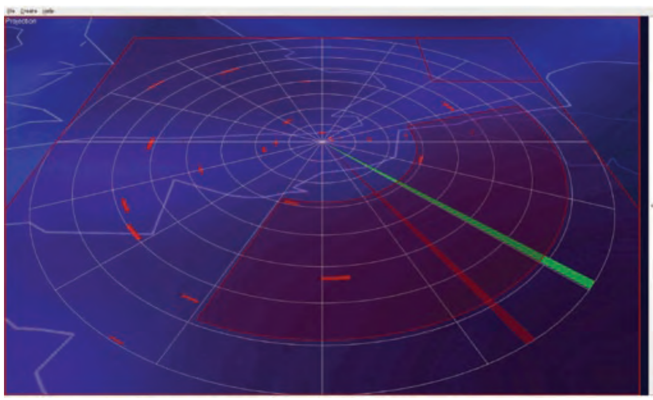

Figure 1

Two-dimensional radar scan conversion is one example of how new levels of system performance can be unleashed using the latent power of the GPU. The same principles can be applied to 3D radar (range, azimuth, and height) where the GPU also provides the ideal platform for displaying the images in many projections and visualizations, able to display a number of them simultaneously on the same screen as well, if required. The use of shader language and the inevitable growth in capability of GPUs generated purely by commercial market pressures appear set to translate into a host of new military battlefield visualization options and performance benefits, truly reinforcing the value of the COTS proposition.

To learn more, e-mail John at john.wemekamp@curtisswright.com.


photo by Petty Officer 3rd class M. Jeremie Yoder, U.S. Navy.

Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

www.mil-embedded.com/dailybriefing

Actel FPGA completes technology boot camp

The RTAX4000S, a “rad-hard” FPGA often found in the ranks of spacecraft payload applications, recently earned its MIL-STD-883 Class B qualification after undergoing hours of rigorous tests: 80,000 hours of life testing and 1,000 hours of High-Temperature Operating Life (HTOL) testing. The 4-million gate FPGA is part of Actel’s RTAX-S family, which has collectively achieved more than 2 million hours of device testing and flight heritage. The RTAX4000S is now progressing toward QML Class Q and QML Class V verification.

U.S. Air Force photo/Staff Sgt. Cassandra Locke

Java-related technology to help brew DIANA’s innovation

Though ideas are already percolating among participants of the European DIANA initiative, mission- and safety-critical solutions provider Aonix was recently chosen to join the effort. DIANA’s forthcoming integrated modular electronics platform will cut operational/development costs of aircraft by modernizing execution environments and tools for safety-certifiable and hard real-time avionics systems; DIANA also promotes and defines common certification processes, strategies, and development. Aonix’s chief role will be to provide virtual machine standards experience and PERC Pico technology, which grants Java’s scalability and portability to low-level software component developers facing stringent memory footprint, performance, determinism, and response time requirements.

CompactPCI to help Navy’s Mercury rise

The U.S. Navy’s E-6B Mercury aircraft will soon soar a little higher (or at least a little better), if Performance Technologies has anything to say about it. The communication systems and platforms developer, in partnership with Rockwell Collins, is slated to give an internal electronics upgrade to Mercury – a strategic command post and communications relay aircraft operating between the National Command Authority (NCA) and U.S. non-strategic and strategic forces. Performance Technologies’ contribution to the project consists of CompactPCI components such as its Intelligent Shelf Manager (ISM), which provides diagnostics and monitoring for remote systems, along with chassis mid-planes and Ethernet switches.

Apache helicopter to “switch” to modernized Ethernet technology

Parvus’ COTS DuraNET 1059 ruggedized Fast Ethernet switch node is reporting for duty in the U.S Army’s AH-64 Apache helicopter modernization program. The device was chosen by the Aviation Applied Technology Directorate (AATD) – a DoD entity responsible for developing, researching, and engineering rotorcraft and tactical UAV technology – in conjunction with a U.S. Army Quick Reaction Capability (QRC) initiative to increase situational awareness. Thirty-four units were ordered by press time, Parvus reports.

NATO photo by NATO Secretary General, Jaap de Hoop Scheffer

Israeli Air Force in a simulated world

Simulation. It’s just *not* the same as being there – or is it? That’s what the Israeli Air Force (IAF) is attempting to find out as it constructs its F-161 Flight and System Trainer. To create virtual terrain for the simulated exercises, the trainer utilizes technology provided by Presagis, including the Lyra image generator, Creator Terrain Studio, Creator Pro, and Creator Virtual Texture Studio. “Accurate and detailed content is vital to the development of realistic, immersive simulations,” says Robert Kopersiewich, Vice President of Product Management at Presagis. The Flight and System trainer will focus on night vision goggle simulations and surface-to-air and air-to-surface weapons delivery training.

NASA astronaut makes appearance at NTS

Photo courtesy NASA/Johnson Space Center

Making a relatively short trek on behalf of NASA, astronaut Jose Hernandez of Stockton, CA – along with representatives from space systems and advanced weapon company ATK – recently recognized National Technical Systems, Inc. at its Santa Clarita, CA test lab. The visit was dubbed a "Human Space Flight Motivational Visit" to reward NTS for its support of the Space Program, particularly for spacecraft launch components' thermal cycling, shock, and vibration testing. Meanwhile, Hernandez was chosen as an astronaut candidate in 2004, then completed multifaceted training by 2006: technical and scientific briefings, land and water survival, physiological training, International Space Station systems and space shuttle training, and T-38 flight instruction. He will complete technical assignments at the Shuttle Branch, supporting Kennedy Space Center Operations, until he is assigned as a mission specialist on a spaceflight.

"One giant leap" for U.S. Air Force missile program

Finishing installation of six COIL (Chemical Oxygen Iodine Laser) modules on the USAF's Airborne Laser (ABL) aircraft might seem like one small step for Boeing and associates; however, the company says it's actually one giant leap for the ABL missile defense program. Boeing Missile Defense Systems VP and general manager Scott Fancher praised the ABL weapon system integration team, indicating that their timely work installing components for the aircraft's high-energy laser leaves the program on schedule for a missile shoot-down planned for 2009. Overall, about 70 percent of laser integration is complete on the ABL aircraft, stationed at Edwards Air Force Base. Laser ground tests and activation will occur sometime after final laser inspections are performed.

CWCEC strengthens its overseas portfolio

Exemplifying the "strength in numbers" mantra, Curtiss-Wright Controls Embedded Computing (CWCEC) recently acquired UK-based ruggedized signal acquisition supplier Pentland Systems Ltd. Accordingly, the acquisition of the Livingston, Scotland company garners CWCEC several technology gains: analog, digital I/O, synchro/resolver, and IF/RF signal acquisition offerings aimed at SDR, radar, and SIGINT applications. The acquisition also builds CWCEC's European and UK market presence, enhancing its existing Letchworth, UK video and integration business unit.

www.mil-embedded.com/dailybriefing

ITAA and GEIA merger:

Union gives stronger voice to government electronics companies

In today's world, everyone wants to be heard, and the high tech industry is no exception. Accordingly, a recent merger linking the Government Electronics and Information Technology Association (GEIA) to the Information Technology Association of America (ITAA) lobbyist organization means the high tech industry's microphone has just been turned up in Washington.

Two-part equation benefits high-tech

The GEIA/ITAA merger makes GEIA its own group within ITAA, retaining the present GEIA board of directors. GEIA will serve as the "back office" of the merger's equation, providing industry standards and intelligence reports that ITAA then powers forward to the government (see sidebar). Frequent ITAA lobbying destinations include the U.S. Congress and agencies such as the DoD, GSA, OMB, and others.

"ITAA was really the logical choice for a lot of reasons. They have very strong government relations, they're very strong in the federal marketplace … and they have an excellent track record as far as representing industry on the Hill," explains GEIA president Dan Heinemeier.

The merger also blends GEIA's 110 members with ITAA's 300. "You got 400 companies in any industry and it's a fairly represented cross-section probably," says Heinemeier. "Our expectation and our hope is that [we] will be more of a first point of contact for the government, when they want to know what the high technology industry cares about as far as policy is concerned."

Another benefit is more member sources for even more robust GEIA reports, he adds.

Charlie Greenwald, ITAA's Vice President, Communications, also anticipates benefits for ITAA members: expanded government relations, increased business development opportunities, access to GEIA's market intelligence, and the opportunity to participate in standards activities.

GEIA and ITAA work together

The GEIA/ITAA merger links these factors:

GEIA: Originated 1950s, www.geia.org

Membership: Companies supplying electronics or Information Technology (IT) to government, including Boeing, IBM, and others

Mission: 1. *Develop industry standards* – The ANSI-certified GEIA standards body focuses on business process standards (for example, setting up a systems engineering program).

2. *Provide market intelligence* – Produces its "10-Year Defense Market Forecast" and "5-Year Federal IT Forecast" reports annually, covering both the defense and nondefense government markets.

ITAA: Originated 1960s, www.itaa.org

Membership: Corporate members, including small IT startups and big players in software, IT services, and the Internet, among others

Mission: To affect change on IT industry issues through governmental lobbying and business networking, concerning: taxes and finance policy, security, workforce and education, online privacy, and more.

Successes, as reported by Greenwald:

- Internet Tax Credit's long-term extension by Congress
- A study/delay of a new government payment withholding tax of 3%

Pending issues:

- Corporate R&D tax credit, which expired in November 2007
- Patent reform
- High-tech immigration (H1B Visas)

Military OS trends you'll want to know about

By Chris A. Ciufo, Editor

For this article, we've done a unique Web 2.0 "mash-up." Answering our call for OS-related *Guest Opinions*, industry responses poured in from commercial, military, and COTS companies. Presented below you'll find (mostly) verbatim commentary from a down-selected group of companies including: **Aonix**, **Concurrent Computer**, **DDC-I**, **Express Logic**, **MapuSoft Technologies**, **MontaVista**, and **RadiSys**. Their unity of thought on topics ranging from Linux to legacy software migration is truly astounding – especially considering how they all play in different markets. Their actual article titles are included to help you gauge their premise and context before you read the excerpts.

For the complete version of each Guest Opinion, check out the April online *Military Embedded Systems* E-letter at: www.mil-embedded.com/eletter/. Of course, if you already subscribe to the newsletter, it'll end up in your INBOX in late April.

Aonix

Real-time Java: Where the rubber meets the road in low-level embedded development

In a world where Java is increasingly considered as the language of choice, having a virtual machine technology with complete application coverage, top-to-bottom, can be a significant advantage. Many embedded Java applications are built using a two-language approach. Java is used for the larger, more complex and more dynamic portion of the application, while C is used for lower-level functionality such as device drivers or portions of the application where faster throughput is required.

Newly available hard real-time Java technologies now make it possible to use the Java language instead of C to address low-level real-time concerns. Compared with the JNI technology, this same hard real-time Java technology also offers superior performance and robustness for connecting traditional high-level Java code to low-level C code. Hard real-time Java can now replace C code for the implementation of device drivers that communicate directly with hardware. This allows a Java-only continuum, ranging from 1- to 10-second response times for full-fledged Java, all the way down to 10 microsecond response times for hard real-time Java, where it's needed to address hardware line speeds.

Concurrent Computer

The value-add of commercial Linux distributions in embedded military applications

Roll your own embedded Linux? It may not be a good idea if you value support, robust tools, and future enhancements. In long-term military programs employing technology upgrades, it's best to stick with a commercially supported distro. If a defense project will require integration of new COTS platforms over time, then the support of a commercial distribution may be desirable to provide maintainability and stability.

The one-stop nature and vendor support of commercial tool kits currently provide a value-add over free, open source tools. The good news for commercial Linux vendors is that use of roll-your-own, in-house tools in embedded projects is down, but the downside is that more developers are using free, user-community, Eclipse-based, embedded tools.

But the 2.6 kernel is still not a true RTOS. Several companies seek to provide value-add by offering kernel enhancements to offer guaranteed real-time performance for applications that consistently need response in the less than 20 microsecond range.

DDC-I

Merging legacy software into contemporary system design

As defense industry software developers transition from Ada to Java and upgrade their hardware, they must do so in a way that protects existing application software. Mixed language development tools that support real-time and safety-critical Java as well as stalwarts such as Ada and C provide a seamless upgrade path that enhances productivity while preserving legacy code.

Military systems typically outlive by decades the technology used in their creation, making it exceedingly difficult to enhance or even maintain the system's capabilities. The problem is particularly acute for software written in the Ada language – once mandatory for military system design. Support for Ada development, in terms of tool availability and numbers of experienced programmers, lags far behind contemporary programming languages such as C, C++, and Java.

A key element for a complete migration solution, then, is a development environment that has the ability to mix legacy languages such as Ada, C and C++, and Java into a tightly coupled solution.

Express Logic

For an RTOS, often "less is more"

The choices include that complex RTOS you've used before, Linux, or a lightweight RTOS that can speed deployment to the field and provide a smaller footprint, making long-life support much simpler. For those systems – those that do not demand hundreds of RTOS services, virtual memory, and the like – a less complex RTOS is often a better fit.

While Linux and complex RTOS products offer attractive capabilities, they might not be the best fit for *all* military applications. Often, a less complex RTOS may be a better choice in the long run. Linux includes hundreds of system services, a process-model virtual memory architecture, and tens of millions of lines of open source code. High-end large commercial RTOS products also include many features and lots of code, making them a challenge to master.

Finally, while Linux is perceived to be "free," the developer must assume the burden of configuration, training, and support, or pay someone else to provide those services. In contrast, *some* military systems demand low-cost development and rapid deployment, and for those systems, Linux or a complex RTOS may not be the best choice.

MapuSoft Technologies

Trends in porting and abstracting applications in military systems

Developers face obstacles in making OS-specific code run on a different OS, designing with changing technologies in mind and host development and simulation. Developers need to leverage their existing software and knowledge base rather than rewrite the software from scratch and throw away the investment made in the development.

Making software written for one operating system run on another operating system is a daunting and time-consuming task with many error prone pitfalls as each OS is different in many ways. A quick example would be the levels of task priorities offered by each OS. Under

standard Linux, for example, the priorities range from 0 to 99; for VxWorks, the range is 0 to 255; for LynxOS, the range is 0 to 512; for Solaris, the range is 0 to 169 priorities.

Developers are looking to utilize OS abstraction tools to write highly portable software that allows for communication among multiple applications across various systems and that negates the need for future rewrites and expensive maintenance. [Such an] abstraction tool should be engineered with safety-critical features vital to defense and mission systems, without sacrificing real-time performance, [as well as] extending features in the future without losing the backward compatibility.

MontaVista

Linux in the military to achieve double-digit growth, but performance is still key

The additional control given by the specific version of Linux depends on the presence or absence of four ingredients in that Linux version. First, if the developer is building a commercial product, they need a Linux with a commercial quality. This will not be provided by source code downloaded from Linux.org. “The kernel.org community is no longer delivering a quality commercial product. It delivers cutting-edge technology and depends on commercial distributions to clean it up and make it into a commercial product.”

The second ingredient is integration. The Linux OS in an embedded device can include the kernel, GNU toolchains, drivers, tools, and applications. The third ingredient is technical support. Embedded developers usually select one version of the kernel and keep it for the life of their device.

Lastly, hardware enablement gives control. A developer’s project will be much more difficult if a commercial-quality embedded Linux is not available for the hardware he needs. You ask, “How portable is the code?” If one distribution supports the boards you need, it is much more portable across different hardware types. If not, it won’t be.

RadiSys

Military systems can benefit by using multicore

Many modern defense systems can benefit from running both real-time and non real-time operating systems. Marrying OS-9 with Windows or Linux on an asymmetric multiprocessing platform requires modern multicore processors such as those from Intel. Virtual machines running on the AMP manage the multiple environments.

This new platform is merging traditional workstations and embedded real-time systems onto one device. It reduces hardware costs, reduces power consumption, and increases system reliability. From a software perspective, the multicore environment provides an efficient platform to create hybrid applications reusing existing software.

In this platform paradigm, Windows and Linux general processing operating systems and a real-time operating system run on separate cores to create a new hybrid, multiprocessing environment. This environment has traditionally existed as separate systems connected through a network to manage front-end real-time control and back-end data management tasks.

An unmanned mobile device or robot providing live video of unexploded ordnance to an operator with an RTOS is an example of where multicore is useful in a military application. The mobile device can also collect additional data for processing against databases stored on a general purpose database on general purpose operating systems like Windows or Linux.

Mission-critical software architecture: FSMs versus RTOS

By Don Carl Berndt

A Real-Time Operating System (RTOS) is a popular selection for critical-mission embedded software architecture. However, software developers should consider a system of Finite State Machines (FSMs) as an alternative architecture.

The use of an RTOS – whether developed "in-house" by savvy individuals or commercially licensed (COTS) – presents difficult issues during the design and coding processes and when performing the independent validation and verification. These issues warrant special consideration in order to provide the reliable and predictable behavior, as well as excellent real-time performance, required of critical mission software. Many of these issues, however, simply do not exist in a system of Finite State Machine architecture. Additionally, an FSM-based architecture provides benefits that will improve upon the design, coding, and verification activities, thereby reducing development costs.

Benefits and design considerations for RTOS-based embedded software

The criteria for selecting a COTS-RTOS for a particular embedded application generally include the following:

- Services provided in the form of an Application Programming Interface (API)
- Scheduling algorithm (preemptive or nonpreemptive) and resulting performance expectations
- Memory requirements for the kernel and stack operations
- Learning curve, customization, and vendor support
- Software development/testing tools and support
- Licensing fees

Many capable vendors offer RTOS products that are suitable for many embedded applications based on these criteria. Vendors are anxious to report their RTOS success stories, and have respectfully met many customers' needs with their useful products. Despite these benefits, however, there are special design, coding, and verification considerations inherent in most RTOSs (COTS and in-house developed) that must be skillfully addressed to ensure a safe, reliable, and cost-effective embedded software product.

RTOS task partitioning and scheduling

Many COTS-RTOS products may be considered derivatives of general-purpose desktop/enterprise operating systems, which, from a processor perspective, execute separate, unrelated applications, referred to as *tasks*. Although this architecture has proven itself sufficient for multitasking desktop operating systems, it may not be the ideal architecture for embedded systems, which typically perform single, high-performance applications.

Partitioning an RTOS-based application into tasks is somewhat arbitrary and usually results in a set of tasks that may be run and tested individually. Tasks are generally constructed as *'while ()'* loops and may use any of the hardware and software resources available to accomplish the required functionality. Figure 1

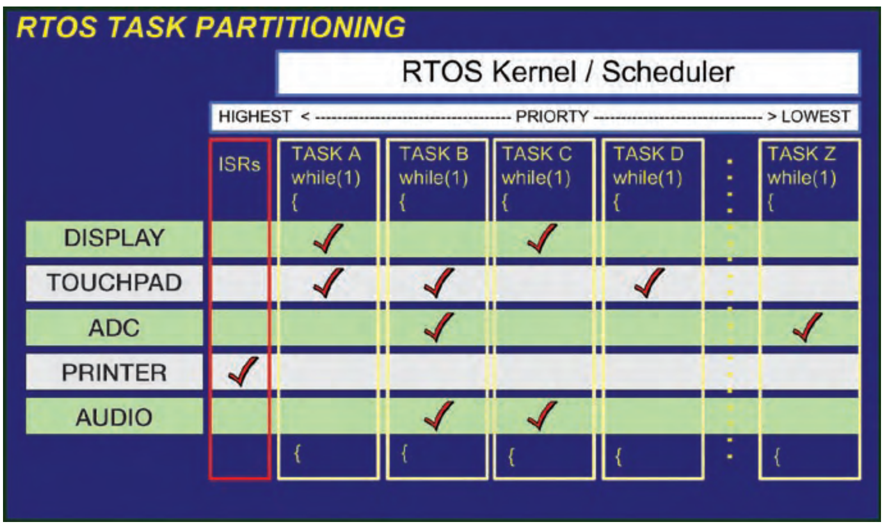

Figure 1

is a visualization of an RTOS partitioning with tasks appearing in columns and typical resources appearing as rows.

Each task is run by a complex and usually proprietary mechanism called the RTOS *scheduler*. This scheduling algorithm may accommodate fixed or dynamic task prioritization to allow all tasks to run at the desired time. This means that each task will be suspended either at a fixed time interval or upon the occurrence of other events, causing another higher priority task to run. A necessary runtime penalty for this scenario is the *context-switch*. This process must occur every time the execution of task is suspended in order to run the next priority task. It involves saving the processor registers and stack for the suspended task, and the restoration of the same for the next task to be run. This operation steals processor cycles from the application code, which might be a consideration for high task switch rates.

RTOS module design and coding considerations

Because each task can be suspended at any time, the task module must be designed and coded skillfully to ensure that proper operation occurs upon resumption of the task. This design consideration is known as *code-reentrancy* and is potentially a significant source of runtime anomalies for RTOS-based architectures.

Another potential pitfall when coding RTOS tasks is the requirement for mutexes/semaphores/tokens to allow for the sharing of resources among RTOS tasks – as though the "right hand knows not what the left hand is up to."

Although RTOSs are currently being deployed in military embedded systems, the inherent characteristics of its architecture require specialized skills to develop safe and effective embedded software. The somewhat arbitrary partitioning of the embedded application into (prioritized) tasks, and the complexity of the task scheduling algorithm, present a difficult architectural framework for software development, test, and debug. The design and coding considerations to accommodate code-reentrancy and resource sharing add additional challenges for developers. An effective verification process will analyze both the RTOS internals and application modules by source-code inspection. The effectiveness of the RTOS scheduler will need to be verified to ensure proper task execution sequences in the dynamic event-driven runtime environment. Theoretically, all possible sequences of events and conditions and the resulting suspension-resumption of tasks must be tested to provide sufficient test coverage for mission-critical software. Software modeling and performance analysis tools may be valuable to the verification process, but the effort to properly configure these tools to obtain meaningful results should be a consideration. Overall, the most difficult challenge might be the comprehensive verification of the RTOS-based architecture and design in order to obtain certification for deployment. Most of these RTOS architectural, design, and coding considerations become nonissues in an FSM-based architecture.

An FSM-based architecture

Because embedded system hardware and software components have a unified purpose in performing a single dedicated function, perhaps a more singular approach to software architecture would be appropriate – specifically, an architecture consisting of a system of individual Finite State Machines. As the use of FSMs has proven itself a worthy tool in the digital hardware design of sequential circuits such as graphic controllers and communication controller ICs, abstracting these powerful concepts into the software realm for embedded systems seems almost intuitive: soft FSMs driving hard FSMs. In other words, it makes sense to design (the layers of) a communication protocol task as a Finite State Machine to 'drive' the communication controller digital device, the design of which is also a Finite State Machine.

Task partitioning as a system of FSMs

Partitioning embedded system software into *application tasks* (versus RTOS tasks) would simply be a matter of *partitioning by resource,* as depicted in Figure 2. In other words, tasks would be responsible for:

- *Driving* both internal and external devices and their interfaces
- Algorithmic data processing
- Data acquisition, storage, and retrieval
- The various layers of communication protocols

Most applications would also require a *control* task, which could provide supervisory control of other tasks as well as

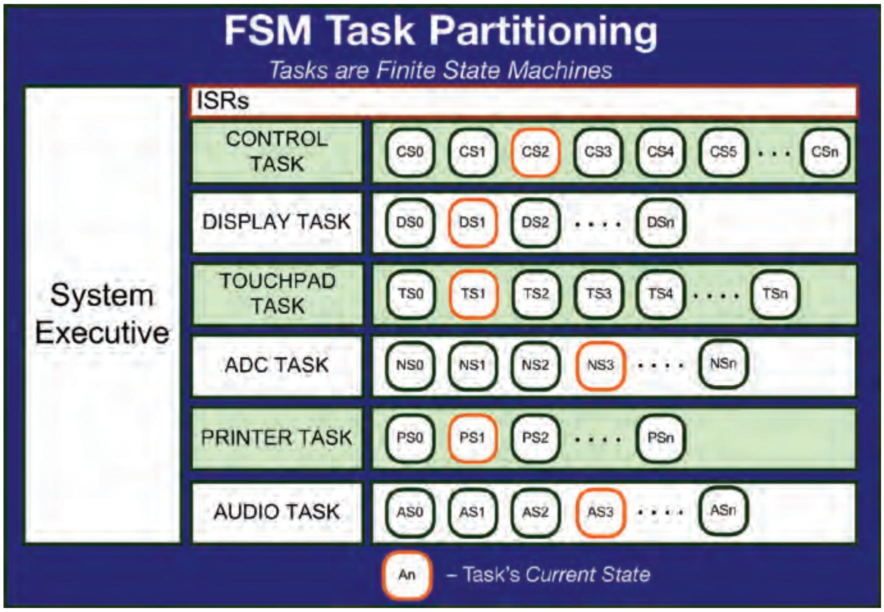

Figure 2

maintaining the *state of the machine,* for example, various modes of operation and/or navigation of a user interface. Additionally, including a task responsible for the detection, reporting, and recovery from errors would likely be a requirement of most mission-critical embedded system specifications.

In this FSM-based software architecture, all application tasks would be designed as individual state machines using conventional state diagrams of the Mealy/Moore paradigm to convey state logic, a template of which is shown in Figure 3. Each state would be directly encoded as a (C-language) function to be *run through* *completion* by a system executive. Each task would maintain its own current state variable to be used by the executive to determine which state function is to be executed for each task. One of the advantages of this method of partitioning is that the issues of context switching, code reentrancy, and resource-sharing among RTOS tasks become entirely irrelevant.

The FSM-based architecture illustrated would also support basic services such as a system timer and intertask communications. In addition to a current state variable, each task could have a timer count that would be decremented by a single timer interrupt ISR. Tasks could communicate using basic messaging and bit flags. Other device interrupts would be handled by device-specific ISRs and possibly setting a flag event for further processing by a particular task.

An FSM-based architecture provides important benefits

The real-time performance of an FSM-based software architecture is superior to that of an RTOS because of the lack of context switching and the inherent nature of state machines. As each task is in a given state at a particular time, if the specified event for that state has not occurred, nothing else needs to be performed for that task, and execution continues with the next task. If the specified event has occurred, processing that event occurs immediately within that state (or subsequent states) and the task's current state variable is updated as required, causing a different state function of the task to be executed on the next pass of the executive. This results in very predictable and deterministic behavior of the entire system, which can be easily measured using basic performance metrics.

Another advantage to an FSM-based architecture is that tasks can be assigned, at design time, to one of many processing elements. The current trend to distribute RTOS/application tasks across processing cores running at low(er) clock speeds to reduce system power consumption is very beneficial but presents challenges to software tool providers. Ideally, to maximize system performance, each processing core could be dedicated to running specific FSM tasks assigned at design time, as opposed to a hardware/software algorithm to dynamically assign (RTOS) tasks during runtime.

The application, as a system of Finite State Machines, can be easily conveyed diagrammatically showing partitioning into tasks, intertask communication, and data flow among tasks. The state diagram for each task is both easily documented and encoded into source modules. As there is no RTOS or scheduler, only a basic executive is needed to execute the current state functions for each task. All of these attributes of an FSM-based software architecture allow the verification process to be more meaningful and easier to perform.

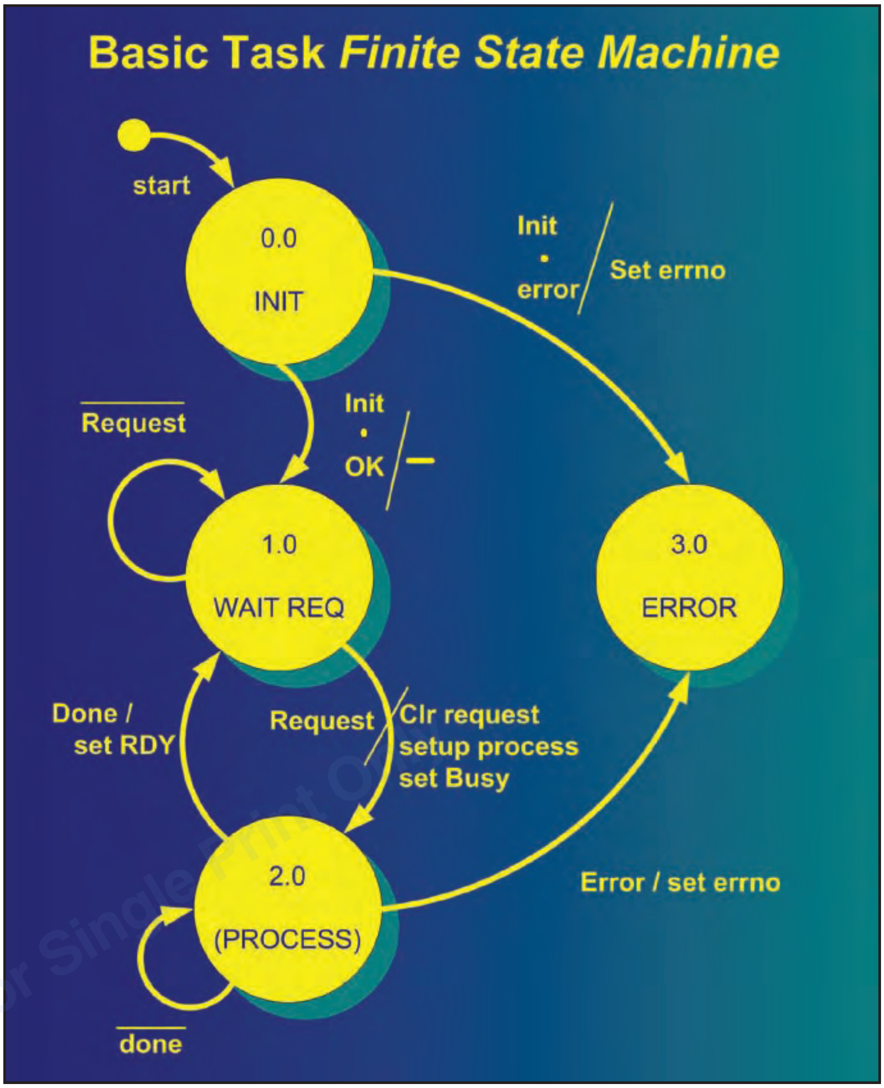

Figure 3

FSM-based architectures for future embedded systems

Embedded system software is deserving of its own architecture and development methods that are more akin to that of hardware design processes, as opposed to those of desktop/enterprise software systems. The use of an FSM-based software architecture would benefit mission-critical applications by providing a consistent design method that can be easily tested and verified. Offering excellent system performance and ease of maintenance, an FSM-based software architecture could significantly reduce the costs and risks normally associated with developing, verifying, and certifying mission-critical embedded software.

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Defining the ultimate rugged PC: Nuts, bolts, and bits

By John Lin

The implementation of computers and computer-controlled devices in combat situations demands that all computing equipment be ruggedized. But what constitutes a rugged PC? Is it simply addressing issues such as impact, vibration, extreme temperatures, dust, and water? Or is there more to it? In today's military applications, data encryption is playing a vital role in ruggedizing the system against battlefield threats – without hindering system performance.

Reliability. It's something everyone wants and expects. As computers play a more central role in military operations and communications, the saying that "failure is not an option" is mandatory when referring to equipment. In combat, any equipment error could be fatal. Military equipment needs to withstand hostile environments with a frenzied mix of foreign objects, extreme temperatures, bumps, and even bullets. At the same time, physical toughness is not all there is to consider. While the application of computers in the military is making the military more powerful, it is also making the military vulnerable in new ways.

Consider the Future Force Warrior uniform[1] system, which sports a wearable computer connected to a network that enables the wearer to have constant communication with command and other soldiers. With the Future Force Warrior uniform system, medics can also keep track of each soldier wearing it from a distance. The networked uniforms allow medics to see via a Web browser the physiological aspects of each soldier (for example, respiration, heart rate, and so on). In addition, commanders can use the system to gain an overall sense of each soldier's location.

The potential impact the uniform system could have on military operations is astounding. Soldiers in the field could have real-time intelligence information and at the same time see real-time satellite images of their target objectives. This gives them a powerful advantage in combat. Back at the base, commanders will likely be able to see live video feeds of the combat zone and assess the need for deploying reinforcements.

However, as with all communications systems, interception is a big problem. If information can be intercepted, no amount of hardware ruggedization should qualify the system for combat use. So what else needs to be done? The data itself needs to be "ruggedized." If the goal of hardware ruggedization is to protect the hardware from hostile environments, then the goal of data ruggedization should also involve protection from hostile environments. The only difference is what constitutes a "hostile environment." For data, one primary type of hostile environment would involve data interception.

Therefore, ideally, data should be masked so that potential data thieves would be completely unaware of any transmission. Practically, obfuscating data is more feasible – that is, to make the data useless if it is intercepted. The key to the latter is knowing where to implement encryption – and knowing how to encrypt without hindering system performance.

Scrambled eggs data

Encrypting data at the application level is a good start, but it is not enough because cryptanalysis can still be performed on the intercepted data. Even throwing in a monkey wrench (for example, adding polymorphic encryption) may not be enough to stop a determined cryptanalyst. What makes data vulnerable? If data were just sitting on an isolated computer, then the data would be safe as long as no one could physically break into the room and access the computer, but the computers in the Future Force System need to be connected to a network. And because all data on a network is transmitted in packets, data protection needs to be reinforced at the packet level.

In the Transmission Control Protocol/Internet Protocol (TCP/IP) model defined by the Internet Engineering Task Force (IETF), when data is broken down into segments at the Transport layer, the segments are assigned sequence numbers so that the data can be pieced back together on the receiving end. The Transport layer is the first end-to-end layer in the TCP/IP model. Therefore, information in the Transport layer header won't be accessed (unless intercepted) until the destination address in the Internet layer header is reached. Anyone capable of intercepting the packets will be able to reassemble the packets.

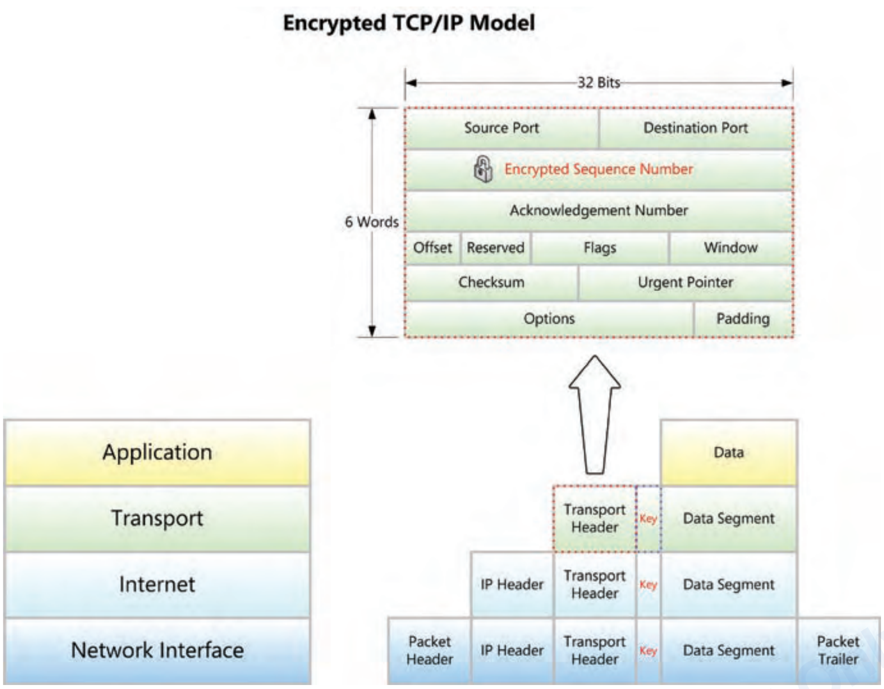

Figure 1

Figure 1 shows an "enhanced" version of the TCP/IP model – dubbed "Encrypted TCP/IP" (ETCP/IP). The ETCP/IP model differs slightly from a generic TCP/IP model in its Transport layer: ETCP/IP adds a special feature to TCP/IP by encrypting the sequence number. The key idea behind encrypting the sequence number is to obfuscate the packet order so that an intercepted message cannot be reassembled. And if someone cannot properly reassemble the packets, then cryptanalysis of the original data cannot even be performed.

Public key cryptographic algorithms, such as RSA encryption[2] (see sidebar), are used as the preferred encryption method because each soldier can have a private key based on the uniform's computer ID, based on biometrics, and so on, so that only they can decode the packet order. Meanwhile, the soldier's public key can be stored on a directory in a secure server so that when data needs to be sent to a specific soldier, the appropriate public key is identified and retrieved for use.

ETCP/IP is based on TCP/IP and preserves the Transport layer header. The Transport layer header is still 6 words (96 bits). However, instead of the data segment immediately following the Transport layer header, the soldier's public key follows at the beginning of the seventh word, after which the data segment follows.

What is RSA?

RSA is an encryption algorithm named after its three founders: Ron Rivest, Adi Shamir, and Leonard Adleman. The algorithm was first published in 1977 in a Massachusetts Institute of Technology (MIT) memorandum. The algorithm is based on public-key cryptography (aka asymmetric cryptography) concepts. Public-key cryptography involves using two keys to encode and decode a message. The public and private keys are related inverses of each other. Having one key enables the verification of the other – somewhat like matching two complementary jigsaw puzzle pieces. An analogy would be an email account. While others may be able to send a message to an email address, they cannot access the contents of the account unless they have the password.

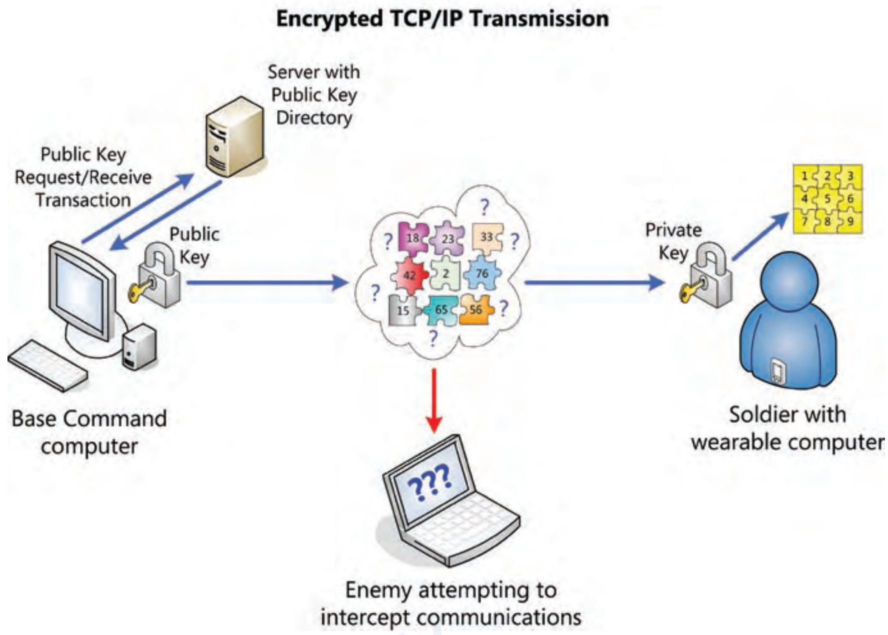

Figure 2

Figure 2 shows an example of what might take place during an attempted interception of an ETCP/IP transmission. The Base Command computer encrypts some data and then sends it using the ETCP/IP communications protocol. When sending the data to the soldier, the Base Command computer automatically requests the soldier's public key and compares it with the last public key used in communicating with the same soldier. Because the soldier's public key should never change, if there is a difference between the public keys, the difference will be recognized as an attempted man-in-the-middle interception.

Even if the attacker successfully intercepts ETCP/IP packets, the attacker will be unable to decipher the contents because the packets cannot be reassembled without the soldier's private key – so the result looks like a corrupted file. When the soldier gets the ETCP/IP packets, the soldier's computer is able to decode the packet order and reassemble the packets in the correct order. Additionally, the soldier can trust that the data is coming from an authentic source because the Base Command computer also has a private/public key pair that is used for signing and verifying each packet.

Rugged data = sluggish system?

Adding the encryption process will require more system resources, and encrypting all transmitted data would slow down a computer noticeably. However, with dedicated hardware handling the encryption and decryption, the encryption process doesn't have to feel like watching molasses drip in winter. Implementing ETCP/IP with software-based encryption would tax the CPU because the CPU is designed to handle instructions generically. A dedicated hardware encryption processor has the instruction set already built-in. Therefore, it can process the instructions much faster.

As further evidence, a comparison between a hardware-based encryption and a software-based encryption is described. The same test system was used to make the test as fair and accurate as possible. The hardware-based encryption used the integrated VIA Advanced Cryptography Engine (ACE) on the C7 NanoBGA2 processor. ACE[3] is a subsystem in the processor that is dedicated to handling AES, SHA-1, SHA-256, and RSA cryptographic algorithms. The software-based encryption relies solely on the processor to handle all instructions in the algorithm. Both are tested using the Microsoft RSA Cryptographic Service Provider (CSP). The comparison shows the performance advantage of using hardware-based encryption.

Software-based cryptographic performance

The processor performed RSA signing instructions with a 512-bit length key at an average throughput of 96.209 kbps. For RSA verification, the processor handled a 512-bit length key at an average throughput of 4.449 Mbps. As would be expected with higher-bit key lengths, data throughput decreases for both signing and verification. When compared with hardware encryption speeds, the performance difference is noticeable.

Hardware-based cryptographic performance

With the dedicated encryption hardware enabled, the processor performed RSA signing instructions with a 512-bit length key at an average throughput of 180.845 kbps – approximately 187.97 percent higher than the software-based performance. For RSA verification with the dedicated hardware enabled, the processor handled a 512-bit length key at an average throughput of 8.064 Mbps – an approximate 181.25 percent higher than software-based performance. When data throughput is compared with software encryption data throughput, it is easy to see the performance benefits of hardware encryption, especially with higher-bit key lengths. (See Table 1, which shows the percentage of performance increase of the data throughput for both signing and verifying when using a dedicated hardware cryptographic processor.)

Bits	RSA signing	RSA verification
512	187.97%	181.25%
1,024	310.00%	246.55%
1,280	350.79%	243.82%
2,048	412.17%	267.19%
3,072	427.02%	263.93%
4,096	451.17%	271.53%

Table 1

A (more) complete definition

Technology holds great promise for increasing military strength. However, without proper considerations for data ruggedness, implementing technology for combat use could backfire. Adding encryption does not have to result in excessively slow data throughput. By using dedicated hardware, performance increase of up to approximately 452 percent over software encryption speeds is achievable. Data ruggedness and hardware ruggedness complement each other. And both are needed for creating the ultimate rugged PC.

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Optimizing multicore SFFs for rugged military environments

By Christine Van De Graaf and David Pursley

> "The idea behind this [multicore] implementation of the chip's internal architecture is in essence a 'divide and conquer' strategy."

Advances and availability of multicore processing platforms have proven to offer higher compute performance, reduced chip count, and lower BOM costs with drastically reduced power consumption. Today, multicore processing capability is being integrated into a number of standards-based modular, off-the-shelf rugged form factors – including COM Express, ETX, CompactPCI, AdvancedTCA, and MicroTCA – each of which has its own benefits and limitations for rugged military applications. Integrating multicore processing technologies, including multi-threading, hyper-threading, and virtualization, is helping these Small Form Factors (SFFs) meet the stringent needs of military applications.

Military applications present engineers with some of the most intense design challenges in the embedded world. Not only do modern military designs demand the ability to withstand extended temperature ranges and high/low pressure (altitude and underwater depth) changes, but their computer boards must also withstand severe shock and vibration elements in these harsh environments – all without sacrificing performance. With the growing need for mobility in the military environment, these applications are now increasingly also requiring reduced Size, Weight, and Power (SWaP) to ensure reliable portability. This eliminates the option to increase the footprint to make room for more power or more performance. To compound the challenge, engineers must meet these stringent requirements often with severe time-to-deployment and budgetary constraints.

At the processor level, the advent of multicore technology has proven to be an attractive option to help conquer these challenges, since it offers the ability to scale applications and add features within embedded form factors without dramatically affecting the energy variables such as thermal output and power consumption.

Explained most simply, multicore processor architecture places two or more processor-based "execution cores" within a single processor. This multicore processor plugs directly into a single processor socket, but the operating system perceives each of its execution cores as a discrete logical processor, with all the associated execution resources. The idea behind this implementation of the chip's internal architecture is in essence a "divide and conquer" strategy. By divvying up the computational work performed by the single microprocessor core in traditional microprocessors and spreading it over multiple execution cores, a multicore processor can perform more work within a given clock cycle. For instance, engineers can integrate controls that previously required separate dedicated systems into one system. This means that only one computer is needed for control and visualization tasks – even for critical and highly complex real-time applications.

Accordingly, designers must be careful to optimize multicore by selecting key system-level features. A strong knowledge of the several SFFs available on the market today also enables designers to utilize multicore effectively.

Technologies to optimize multicore processors

With the proliferation of multicore offerings, it is important to keep in mind that not all multicore platforms are created equal. To maximize the capabilities of multicore technologies, a number of key system-level features must also be available. The platform approach from Intel for multicore processing combines a multicore architecture with complementary system-enhancing technologies to enable developers to leverage the architecture very efficiently. These multicore technologies include:

- ***Thread-level parallelism*** – In order to take full advantage of multicore processing performance, both the operating system and applications running on the computing platform must support a technology called *thread-level parallelism*. A processor equipped with thread-level parallelism can execute completely separate threads of code. This allows one thread running from an application and a second thread running from an operating system, or parallel threads running from within a single application.
- ***Hyper-Threading Technology*** – Multicore capability reflects a shift to parallel processing – a concept originally conceived in the supercomputing world. Hyper-Threading Technology (HT Technology) enables processors to execute tasks in parallel by weaving together multiple "threads" in a single-core processor. Whereas HT Technology is limited to a single core's using existing execution resources more efficiently to better enable threading, multicore capability provides two or more complete sets of execution resources to increase compute throughput. This increases the amount of work a processor can do in the same time as a processor with one core. With HT technology, one dual-core processor is able to simultaneously run four software threads. As more processors are added to a server, the number of supported threads increases to help deliver better overall performance.
- ***Virtualization*** – Another important feature is Virtualization Technology (VT), which allows multiple operating systems and applications to run as "virtual machines" in independent partitions on one platform with simpler hardware administration. This makes overall systems more stable because processes that would collide on single-core systems can be separated. The partitions can be assigned as necessary, even when the system is running. VT offers the option to integrate previously stand-alone systems such as controllers, firewalls, and data servers, completely isolated from each other in a single system. Multicore and VT together offer innumerable configuration possibilities and a degree of freedom for implementing multiple applications on one system, which ultimately leads to savings in hardware.

Future-proofing multicore designs

While the current generation of embedded processors consists of dual-core processors, multicore processors are the goal as technology shrinks and more real estate is available on the die. Quad processors are only the beginning. Chipmakers will continue to push for greater performance, using a combination of improvements in circuitry and more advanced manufacturing technologies. Multi-threaded software can take advantage of existing and future processor designs. For example, if an application has been set up for hyper-threading, it can deliver immediate benefits on a dual-core system because it is already written to utilize two threads. However, if developers architect programs for as many threads as possible within the program, as additional cores become available the application will run faster and more efficiently. The practice of threading beyond the immediate number of available cores can help to future-proof the design.

Embedded SFFs utilizing multicore

Until recently, VME was the solution of choice for high-end military applications. However, current VME designs are unable to meet some of the new application demands due to beyond-budget price points, high power dissipation, and relatively large size. To satisfy the need for smaller size and lower cost, a number of standards-based, modular, off-the-shelf rugged form factors have emerged and are utilizing multicore processing technology: COM Express, ETX, CompactPCI, AdvancedTCA, and MicroTCA. Each has its own variables of size, performance, power dissipation, and price points to consider, providing a wider range of options for military applications. (See Table 1 for a comparison.)

CompactPCI

CompactPCI has thrived in the military market, since the limitations of VME-based architectures have been unable to keep up with the requirements. The 6U form factor has quickly replaced VME in large custom designs. But as the pressure to reduce size and weight intensifies – particularly for Unmanned Aerial Vehicles (UAVs) that carry an increasing array of electronics – the smaller 3U CompactPCI is gaining popularity. The 3U form factor also offers ruggedization benefits due to its significantly greater stiffness, making it less susceptible to shock and vibration.

AdvancedTCA

AdvancedTCA, with its high bandwidth and design flexibility, has also made significant in-roads within military communication applications that are not in the conflict zone. Targeted to the requirements of next-generation carrier-grade communications equipment, AdvancedTCA incorporates the latest trends in high-speed interconnect technologies, next-generation processors, and improved reliability, manageability, and serviceability.

MicroTCA

MicroTCA is a relatively new PICMG standard for open modular systems and preserves many of the important philosophies of AdvancedTCA, including the basic interconnect topologies and management structure. Whereas AdvancedTCA is optimized for very high-capacity applications, MicroTCA is designed to address cost-sensitive and physically smaller applications with lower capacity and performance requirements. By configuring highly diverse collections of AdvancedMCs in a MicroTCA shelf, many different applications can be easily realized.

The Kontron OM6040 is a compact and modular MicroTCA platform that is ideally configured for the design of small, compact, and highly integrated multiprocessor systems based on either PCI Express (PCIe) or GbE packet switching backplane technologies. The small, packet-switched backplane system is an optimal choice for telecommunication applications for demanding military networking environments including interoperable integrated MicroTCA and WiMAX solutions for fixed wireless, last-mile wireless, back-haul capabilities, and cellular for military vehicles.

Form factor	Size (mm x mm)	Key features	Potential applications
3U CompactPCI	100 x 160	Compact size and weight; rugged design	Avionics (such as UAVs), graphics-based ground applications
AdvancedTCA	322 x 280	Fast bandwidth; design flexibility; open framework	Next-generation carrier grade communications equipment (such as communication servers)
MicroTCA	73.5 x 181.5	Modular; compact size; flexible; efficient cooling	Next-generation mobile network applications
ETX	95 x 114	Customizable; rugged	Avionics, rugged computing platforms (such as UMPCs)
COM Express	125 x 95	Small, rugged, flexible	Unmanned vehicles, training simulators, portable tactical communication devices

Table 1

ETX

Embedded Technology eXtended (ETX) has established itself as a popular non-backplane form factor. Targeting customizable embedded requirements, ETX modules offer reliable operation and a long life even in harsh environments. ETX modules employ heat-spreader plates to create a larger surface area over the module to assist with conduction cooling, making these COM modules an option for use in extended temperature ranges as long as the components in the design can tolerate the harsh environment.

ETX modules have been successfully implemented into rugged ultra-mobile PC applications that demanded a modular design with great flexibility. The photo on page 28 shows a small, rugged, and portable device that was designed quickly using a semi off-the-shelf solution along with custom BIOS. In this application, ETX modules, like the one shown in Figure 1, provided maximum performance that allowed the mobilized system to fulfill the demand for mission-critical, high-end computing.

Figure 1

ETX modules have also proven successful in avionics where shock and vibration are among the greatest issues. Through the small, space-saving design of an ETX CPU module, many space-restricted applications can benefit. ETX modules, specifically the ETX-CD and ETX-PM derivatives, have also proven ideal for custom designs involving computing modules in mobile platforms.

COM Express

Small and rugged, Computer-on-Module implementations are ideal for a broad range of embedded applications where they fit mechanically, economically, and functionally, and where other form factors

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such as add-in cards cannot be used. High-performance segments can use COM Express modules to help transition designs reliant on legacy bus technologies to future-focused technologies such as PCI Express and Serial ATA. The form factor flexibility of COM Express with its five pin-out types enables developers to segment their designs for different classes of embedded applications. Applications such as unmanned vehicles, training simulators, and portable tactical communications devices can all benefit from the COM Express form factor.

Multicore SFFs meet current and future needs

Multicore processor-based small form factors offer a variety of attractive choices for today's rugged military applications with their ability to meet the military's increasing SWaP demands, while also holding a promising future for evolving requirements. Accordingly, thread-level parallelism, hyper-threading technology, and virtualization are key to this equation. As a result, the number of architectures that can stand up to the demands of military applications has grown and offers many performance, size, and cost alternatives to choose from. As new technologies come to market, even more powerful computing platforms are on the horizon.

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David Pursley *is a field applications engineer with Kontron. He is responsible for business development of Kontron's MicroTCA, AdvancedTCA, CompactPCI, and ThinkIO product lines in North America and is based in Pittsburgh, PA. Previously, he held various positions as a field applications engineer, technical marketing engineer, and marketing manager. David holds a Bachelor of Science in Computer Science and Engineering from Bucknell University and a Master's degree in Electrical and Computer Engineering from Carnegie Mellon University. He can be contacted at david.pursley@us.kontron.com or 412-919-3709.*

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Do more with less: Designing a PowerPC SBC for low-power applications

By Manville Chan

Do more with less" is a mainstay mantra in most design directives, causing hardware design engineers to make a trade-off between high performance and low power consumption. Manville describes some steps that will help lower PowerPC SBC board power consumption, thus mitigating the trade-off.

The Power Architecture (also called *PowerPC*) is known for its open-source architecture, real-time/deterministic capability, high performance, relatively low power consumption, and long-term component availability. As a result, it is a popular choice for a number of compute-intensive military embedded applications such as signal processing and electronic warfare.

Today, designing a PowerPC-based SBC has become more challenging, as hardware engineers often need to make a trade-off between performance and power consumption. In many cases, the faster and more powerful the processor, the more wattage it dissipates. As more heat is generated, the hardware becomes less reliable under harsh environments. The enclosure thermal design becomes bulkier, pricier, and more complicated.

To meet this challenge, steps can be taken to lower power consumption in high-performance PC SBC designs, including processor selection and choosing the right bridge controller. Details such as the efficiency of Point-Of-Load (POL) DC-DC converters, pull-up resistors, and reducing LED power draws also help to reduce SBC power consumption. (For clarification, high-performance PowerPC processors are defined herein as those with SIMD vector processing engines such as AltiVec, suitable for compute-intensive military intelligence applications.)

Selecting the right processor

Selecting a processor is obviously the first and the most important step in lowering overall power consumption. A number of semiconductor manufacturers, including Freescale, P.A. Semi, IBM, AMCC, and Xilinx, provide PowerPC processors that vary in features and performance. Unfortunately, there are no governing bodies or test laboratories validating power consumption specifications published by these manufacturers. So, design engineers are often faced with apples-to-oranges comparisons when it comes to evaluating power consumption among manufacturers. Reference boards could help engineers to better determine actual power dissipation for their application, but most engineers can rarely afford the time to evaluate each solution one by one. Figure 1 compares the typical power ratings of the most popular PowerPC processors.

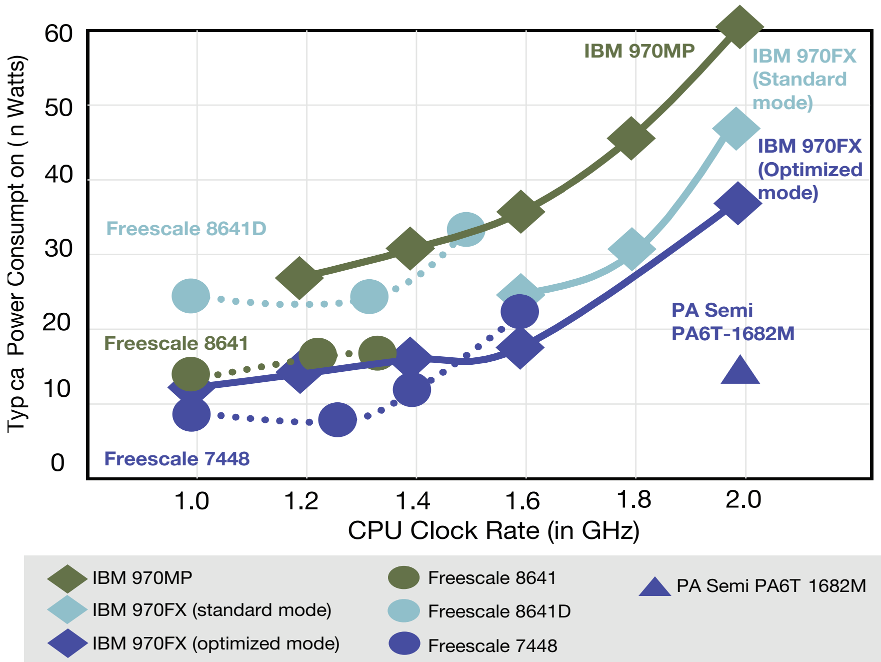


Figure 1

In most instances, an integrated System-on-Chip (SoC) processor offers lower overall power consumption since it eliminates the need to use additional bridge controllers to interface with memory and I/O. In the past, integrated SoCs, such as the original Freescale PowerQUICC architecture, provided higher integration but lower processor performance. However, today's integrated SoC performance is comparable to or exceeds that of a discrete processor implementation. P.A. Semi's PA6T-1682M and Freescale's 8641/8641D are all high-performance PowerPC processors with integrated memory and I/O controllers.

If the design requires the use of multiprocessor technology, design engineers may now choose between placing multiple single-core processors and using multicore technologies. Multicore solutions typically provide power savings over using multiple single-core processors. The IBM 970MP, P.A. Semi PA6T-1682M, and Freescale 8641D are examples of dual-core, PowerPC processors available today. However, the use of dual-core technology is still not in its prime. Real-Time Operating System (RTOS) support for multicore is still in its infancy. Exacerbating the problem is the fact that dual-core processors can have different memory architectures; for example, some use shared memory whereas others use distributed memory. This makes RTOS support very difficult.

Once a processor vendor and device family are chosen, it's important to select the correct device and operating parameters to optimize power consumption. In many cases, a small reduction in the maximum core clock rate will allow a device to be supplied with a lower core voltage, providing a very significant reduction in power. For instance, a popular version of the Freescale MPC7448 runs at up to 1.267 GHz with 12 W maximum power. The same part can run at a lower core voltage at up to 1 GHz for only 8.5 W maximum power. After adjusting for point-of-load efficiency, that 3.5 W is nearly 8 percent of the power budget for a typical SBC with a total maximum power consumption of 46 W.

It's also important that the hardware and software allow the user to reduce the core clock rate, when desired, and to use other power management features of modern processors. Hooks should be provided in the Board Support Package (BSP) that makes application-level power management easy to implement.

Beyond the processor selection

The processor's core power consumption is often only 20-40 percent of the total board power consumption. Good design practices can minimize the power dissipation of a processor's surrounding circuitry.

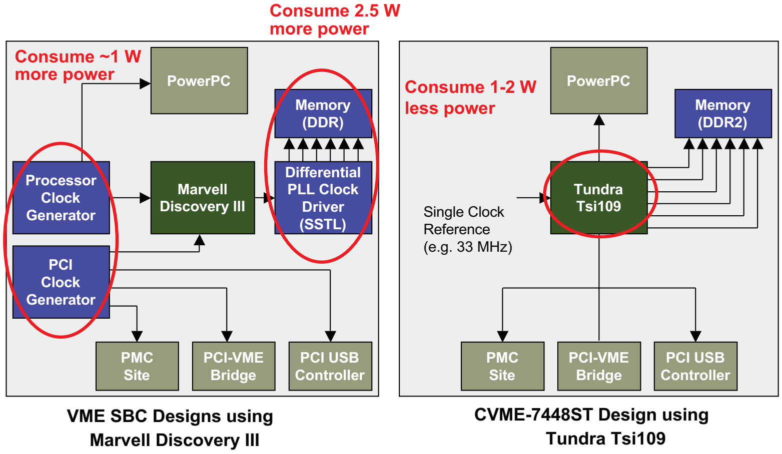
For a discrete CPU design, choosing the right bridge controller is the first logical step after processor selection. Thanks to the open source Power Architecture community, engineers have more choices for bridge controllers than Intel designers do. A number of manufacturers – such as Marvell Semiconductor, Tundra Semiconductor, and IBM – offer processor controller devices. In a recent Cornet Technology VME SBC design, switching to a Tundra Tsi109 controller saved approximately 6 W – or about 13 percent of the total board maximum power consumption of

46 W (see Figure 2) – over a previously used controller. Part of this power savings comes from utilizing a newer generation of memory interface technology, eliminating the need for external signal terminations.

Secondly, the efficiency of the Point-of-Load (PoL) DC-DC converters can be a very significant factor in the total power consumption of an SBC. Generally, devices with higher switching frequencies are more efficient than linear converters at the expense of some extra real estate. Due to design complexity and EMI issues, integrated switching power modules should be strongly considered. It is also important to ensure that the PoL devices are operating in a "sweet spot" in terms of current loading to maximize efficiency. Figure 3 shows the efficiency versus load current for a typical PoL DC-DC converter. The efficiency "sweet spot" for this particular device is between 2-6 V.

Thirdly, pull-up resistors with higher values can significantly save on power consumption. Even though the current through each pull-up resistor is typically low, the total current being drawn can be high. Moore's Law and the miniaturization of integrated circuits allow for more logic and more signals in a single PCB, potentially requiring more pull-up resistors. Two hundred 1 KOhm pull-up resistors to 3.3 V consumes over a watt of power when their signals are driven low 50 percent of the time. If these can be changed to 10 KOhms, the power savings is an order of magnitude or tenfold. Board design engineers should pay attention to the minimum current requirements for each signal and each device and then select the largest resistor value possible.

Lastly, reducing the current draw by LEDs will also lower power consumption. This is especially true for designs using a large number of LEDs. Some bright LEDs can draw over 20 mA of current, increasing the overall power consumption by 1 W per 15 LEDs in a typical application (3.3 V at 20mA). Choosing from the growing number of LEDs that use advanced semiconductor technologies to provide a high luminescence for minimal power (~ 50 lumens/W, depending upon color), is one way to keep power low. LED brightness requirements can be determined in the prototyping stage, enabling current-limiting resistors to be adjusted as needed in the final configuration. Depending on design needs, debug LEDs can also be removed to save additional power.



Using Tundra Tsi109 over Discovery III	1 2 W
Using DDR2 to eliminate SSTL design	2 5 W
Eliminating external clock generators and clock buffers	~ 1 W
Total Power Savings:	**4-6 W**

Figure 2

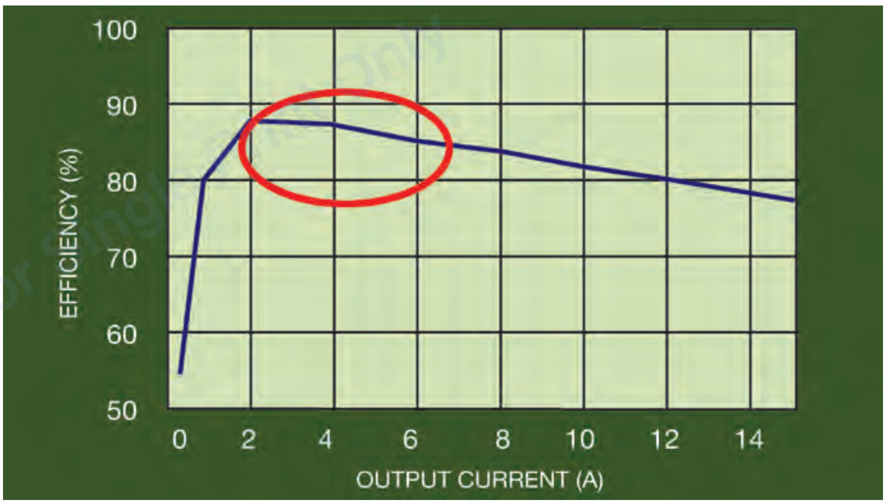


Figure 3

Final analysis: The energy economist

Designing a high "performance-per-watt" PowerPC SBC can be as much art as it is science. Board design engineers are becoming macro-economists by looking at the larger picture and making energy policy decisions rather than individual implementation choices. It is only by analyzing real-world system performance that processors and parameters can be determined in the interest of balancing performance and power. Furthermore, by researching alternatives for bridge controllers and DC-DC converters, as well as paying attention to the smaller details like pull-up resistor values and LED power draws, it is possible to lower the overall power consumption to compensate for today's high performance, power-hungry processors.

Manville Chan *is program manager at Cornet Technology, where he's responsible for the company's high-performance embedded computing products. Previously, he was a product marketing manager at SBS Technologies, responsible for the mezzanine I/O module product line. He holds a BS in Computer Science and a BS in Advertising from the University of Texas at Austin and an MBA in International Management from the Thunderbird School of Global Management. He can be contacted at m.chan@cornet.com.*

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Leveraging the synergy of Software Product Line engineering and Model-Driven Development

By Charles W. Krueger, PhD

Developing software for a portfolio of similar products is a formidable task, but Software Product Line (SPL) engineering effectively addresses this challenge. Model Driven-Development (MDD) raises the level of programming abstraction with UML, to make software engineering more efficient. Integrating MDD and SPL techniques results in a simple, elegant approach that enables organizations to effectively manage product line diversity in MDD for faster development of more new products and features.

The motivation for integrating Model-Driven Development and Software Product Line engineering is to capitalize on the strong synergy that results between the two. MDD is well known for its ability to accelerate system and software development by leveraging the higher level of abstraction provided by UML and SysML rather than conventional programming languages. SPL engineering provides the ability to efficiently and effectively create, maintain, and evolve a portfolio of similar products by taking advantage of a very strategic and predictive form of software reuse. By combining these synergistic technologies, an entire product line can be expressed and engineered from a single configurable MDD model.

MDD and what can be gained from SPL

MDD technology enables professionals to achieve productivity gains over traditional programming language approaches by enabling users to specify the system design and architecture graphically with the UML and SysML modeling standards, and to simulate and automatically validate the system as it is being built. This allows engineers and developers to more rapidly produce a systems specification that is correct, unambiguous, and satisfies the original requirements.

With MDD, creating software for a portfolio of similar products has traditionally relied on one of two different approaches, *clone-and-own* or *one-size-fits-all*. In the clone-and-own approach, new products are created by copying and modifying existing products, as illustrated in Figure 1. The model for each of the products – A, B, C, D, and E – is shown as a circle. After the original product A is created from scratch, each new model is created by making a copy – or clone – of a similar model and then modifying it to implement the unique features and characteristics (shown as diamond, star, and triangle) of the new product. For example, product B is created by cloning product A, illustrated by an arrow, and then modifying the clone with the customizations illustrated as a star. Similarly, product E is created by cloning and modifying product B.

There is 100 percent reuse at the time of cloning, but similar to clone-and-own of conventional source code, the duplication leads to divergence over time and requires merging or replicated development among the different models, adding to the time and cost of maintenance and evolution.

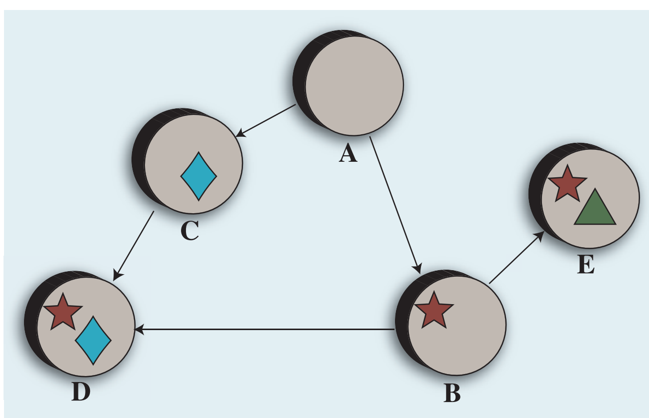

Figure 1

Some organizations adopt the one-size-fits-all approach to avoid the overhead of clone-and-own, as shown in Figure 2. With the one-size-fits-all approach, the product diversity for an entire product line portfolio is implemented in a single model, shown as the same diamond, star, and triangle from Figure 1, in a single model. Conditional constructs in the model, shown as question marks, express decisions about which optional features to include or exclude in any particular product. Similar to one-size-fits-all in conventional source code, this approach can lead to models that continue to grow larger and more complex over time as more and more products and features are added to the portfolio.

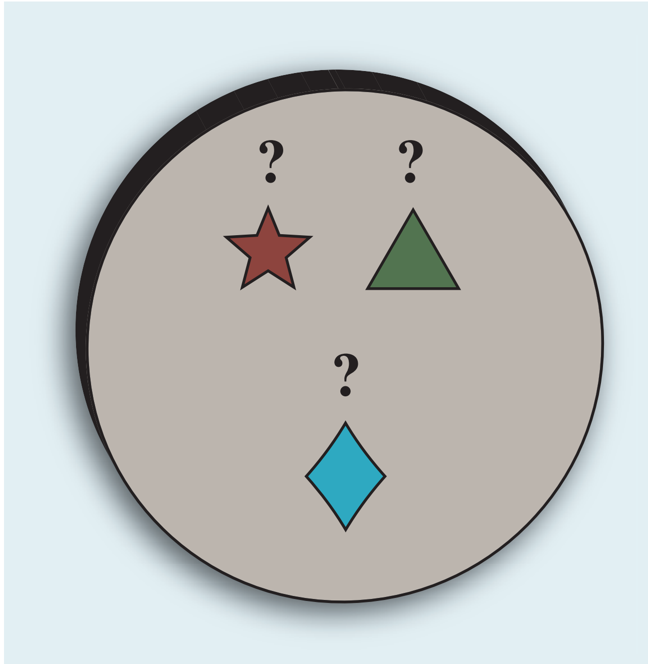

Figure 2

SPL and what can be gained from MDD

The software product line problem can be characterized as a mismatch problem. Customer demand requires most companies to create a product line portfolio of similar products rather than just a single product. The software for these products must be developed to support the feature and function diversity within the product line. However, most of the software development methods, tools, and techniques in the industry today take a product-centric approach. The product-centric approach focuses on how to take a single product through the development life cycle – from requirements through design, implementation, and test – and does not provide explicit and effective support for developing a product line portfolio.

Case studies show that using product-centric tools and methods for SPL engineering can account for 50 to 90 percent of the total software development cost and effort. SPL approaches provide new capabilities for eliminating this overhead waste.

With SPL engineering, specialized tools and methods are provided for efficiently creating, maintaining, and evolving software assets for a product line portfolio of similar products. A high degree of software reuse is possible within the well-defined architecture of a product line.

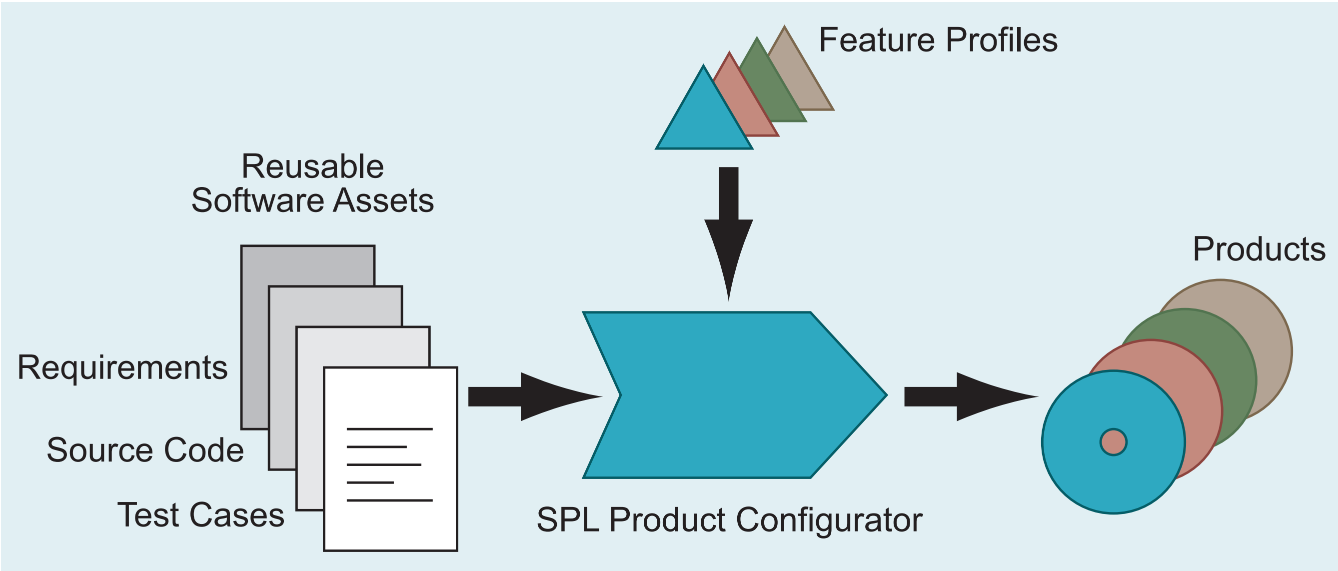

Figure 3

Figure 3 illustrates the *SPL* approach. The SPL product configurator takes two types of inputs – reusable software assets and product feature profiles – to automatically create the individual products within a product line portfolio. The reusable software assets contain variation points to encapsulate implementation-level diversity needed for the product line. The product feature profiles characterize feature differences and selections for the different product instances in the product line portfolio, analogous to an options list for optional and alternate features that are available on a new car. (See the Fall 2006 issue of *Military Embedded Systems*, page 39, for a more detailed introduction to *The emerging practice of software product line development*.)

In the past, SPL tools and methods have primarily focused on conventional source code, requirements, and test cases. SPL support has not been available for variation points that capture product diversity in UML and SysML model elements in the MDD paradigm. SPL support has not been available to allow MDD models to serve as reusable SPL software assets that can be automatically configured by an SPL product configurator.

Bridging MDD and SPL

With the increased adoption of SPL and MDD technology throughout the software industry, the need for these approaches to interoperate has likewise grown. A team of SPL and MDD experts from BigLever Software and Telelogic recently teamed up to explore the idea of integrating SPL and MDD technologies. The results of this collaborative effort illustrate a bridge between MDD and SPL.

MDD/SPL integration provides the combined simplicity and benefits offered by the MDD and SPL approaches – including significant gains in productivity, reduction in defect density, and faster time-to-market with new products – as well as synergistic benefits that increase the product line portfolio's scalability.

On the SPL side of the MDD/SPL bridge, UML models can now be first-class SPL reusable software assets in a product line. Referring back to Figure 3, these model assets can now be interspersed with other types of reusable software assets such as requirements, source code, and test cases. The SPL variation point concept is extended to include MDD model elements to express model diversity in the model elements. Automated product configuration in SPL now extends to include automated

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configuration of different model instances based on feature selections in the SPL feature profile for a particular product.

On the MDD side of the MDD/SPL bridge, UML and SysML models explicitly show both the common and varying parts of the product line design. Each SPL variation point's design – including the options, alternatives, and the logical specification that differentiates them – is directly visible in the model. This allows optional elements and alternative behaviors to be specified for model elements, where the options and alternatives reflect the feature diversity that needs to be supported in the model.

The approach offered by an MDD/SPL bridge provides the benefits of consolidation offered by the one-size-fits-all approach and the benefits of precise customization offered by the clone-and-own approach, without the associated drawbacks. When the SPL product configurator configures all the variation points in an MDD model to produce the model for a product, the result is the precise model needed – nothing more, nothing less.

Leveraging the synergy for business advantage

Companies face complex challenges when creating and maintaining the software needed to support a rapidly expanding product line portfolio. To better address this challenge, an MDD/SPL bridge solution converges the synergistic MDD and SPL approaches. With this integration, development organizations can achieve dramatic productivity gains and heightened efficiency. These tactical engineering benefits enable companies to deliver more new products and features faster, while optimizing product quality. The resulting strategic business benefits are large enough to change the fundamentals of how companies compete.

Charles Krueger, *PhD, is the founder and CEO of BigLever Software and has 20 years of experience in software development practice. He has led commercial software product line development teams and helped companies – including Salion, 2004 Software Product Line Hall of Fame inductee, and LSI Logic, 2006 Software Product Line Hall of Fame inductee – establish software product line practices. He is the author of more than 30 articles, columns, and book chapters. He is also a frequent organizer and speaker for the International Software Product Line Conferences and moderates the SoftwareProductLines.com practitioner community website. He received his PhD in Computer Science from Carnegie Mellon University. He can be reached at ckrueger@biglever.com.*

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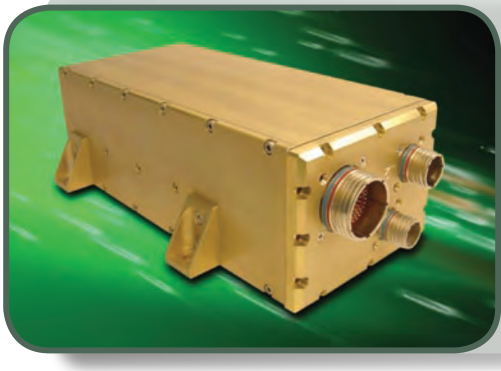


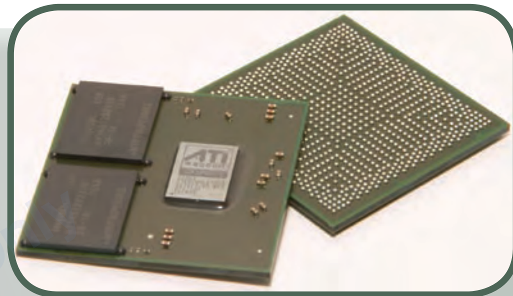
Flexible, rugged two-slot CompactPCI shoebox

We've said it for years: Conduction-cooled 3U CompactPCI is an ideal form factor for small spaces, especially for military retrofits. Rugged supplier Aitech completely agrees. Their E192 modular enclosure is lightweight (relatively speaking), sports a removable and modular PSU, and is completely sealed for harsh mechanical, chemical, or EMI environments.

The box houses a two-slot backplane for ANSI/IEEE 30.1-2002 conduction-cooled 3U CompactPCI and PMC modules. The conduction-cooled cold plate chassis design can dissipate over 50 W at 71 °C while maintaining a maximum 14 °C at the card edge. The MIL-STD-704 PSU provides 28 V, and other options are available. A backplane transition module supports custom front panel connections, typically for circular MIL-C-38999 connectors.

Aitech Defense Systems • www.rugged.com • RSC# 34304

Desktop graphics focuses on embedded



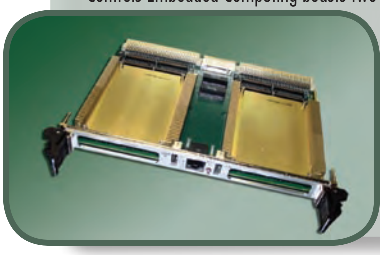
While graphics chipset supplier ATI concentrated on PC desktops and gaming rigs, ATI-owned-by-AMD is looking a bit deeper into the embedded space. Long a player in embedded systems, AMD is targeting the ATI Radeon E2400 graphics processor at test and instrumentation, point-of-sale terminals, kiosks, ATMs, gaming consoles, and yes – even defense applications. Even better, similar to Intel's embedded plans, AMD will back up their embedded support with a five-year availability promise, extra reliability, and other long-term support so essential in purpose-built embedded platforms.

On the technology side, the E2400 is a 65 nm device that supports Microsoft's DirectX 10, 2D and 3D graphics, and multimedia loading. There's 128 MB of on-chip GDDR3, which saves precious board real estate by eliminating external memory. There's even a graphics PCB module called the MXM-II with 256 MB of GDDR3 DRAM that can either be used as a lab mule, or deployed in end-user applications.

Advanced Micro Devices • www.amd.com • RSC# 35885

"It's two, two, two ... cores in one!"

So OK, the title's a bit silly but seeks to illustrate what you knew was inevitable: two dual-core Intel CPUs on the same board. In this case, the SVME-1900 from Curtiss-Wright Controls Embedded Computing boasts two independent ultra-low voltage 1.67 GHz Intel Core Duo processors. This air-cooled 6U VME SBC also boasts dual PMC expansion sites with front panel I/O.

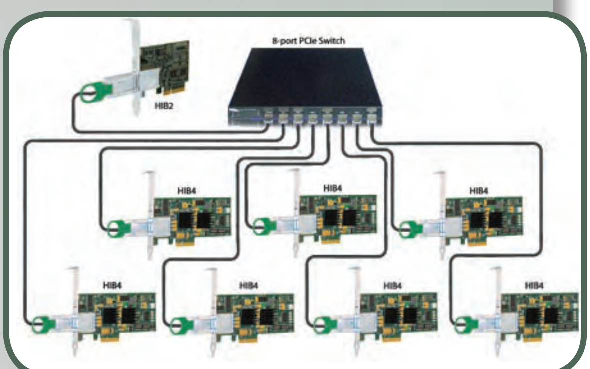


Other specs for this board include 2 GB of DDR2 SDRAM with ECC, 2 GB of USB user flash formatted as two individual USB drives, and the Intel E7520 Memory Controller Hub (MCH)/6300ESB I/O Controller Hub (ICH). For I/O, there are two 10/100/1000 Ethernet ports, 4 USB 2.0 ports, 12 serial ports (4 RS-232; 8 RS-422), 2 SATA ports, and ... wait for it, 12 digital I/O lines. As always, CWCEC's products are available in a variety of ruggedization levels, and the company's Guardian Select life cycle maintenance services are darned near essential for military and long-life programs.

Curtiss-Wright Controls Embedded Computing • www.cwcembedded.com • RSC# 35579

Ethernet? *Nope.* 10 Gbps host-to-host transfers via PCIe

The beauty of PCI Express is not only its speed, but how this desktop technology is becoming ubiquitous and inexpensive. With its low overhead and efficient protocol, PCIe might make a better way to link host computers together than simply using Ethernet. Even better – PCIe supports cable connections up to tens of meters long. One Stop Systems, a provider of industrial-strength communications and computing products, is banking on PCIe as a replacement for Ethernet (or InfiniBand) in ultra-high performance host computers. The company's SuperSwitch family allows communications via PCIe between two, five, or eight compute nodes.



Comprising a PCIe x4 Express Card or a PCIe card, x4 cables, and a switch, the SuperSwitch family includes everything needed to connect host machines. The ExpressNet software manages the interfaces, handles the protocols, and keeps the 10 Gbps connections humming. Switches come in a variety of form factors, including CompactPCI, mezzanines, or 1U sizes. The 1U SuperSwitch 3 has eight ports and can scream along at an astounding 40 Gbps. Ethernet can't even come close.

One Stop Systems • www.onestopsystems.com • RSC# 36156

Explosion- and water-proof computer

Whether on the battlefield, at the depot, the supply dump, or in the ordnance magazine, explosion potential is deadly serious business. That's why the Ruffneck Zone 1 Explosion Proof Computer from Computer Dynamics (a GE Fanuc company) might be the way to go for peace of mind. Equipped with an Intel Pentium M 1.6 GHz single board computer inside, the box is designed in compliance with Europe's ATEX (from the French: ATmospheres EXplosibles). Zone 1 compliance defines an area where the chance of explosion can exist for short periods of time, but an explosive atmosphere won't accumulate for more than a total of 1,000 hours within a 12-month period. The system is also certified for a UL HAZLOC (hazardous location) environment.

The direct sunlight readable 15" (diagonal) LCD is impact resistant, supports bare- and gloved-hand operation, and includes software dimming for darker environments. The SBC supports 2 GB of DDRAM, a 40 GB HDD, optional CompactFlash SDD, and Ethernet or Wi-Fi. There's a watchdog timer, and the Ruffneck runs Windows XP. Designed to operate over -40 °C to +60 °C with optional heaters, the NEMA4 enclosure can be hosed down for HAZMAT operations. The Ruffneck weighs only 45 pounds plus the yoke or arm mount. With this computer, you *won't* be blown away. That's a good thing.

GE Fanuc Intelligent Platforms • www.gefanuc.com • RSC# 34427

Battery- and cable-free wireless sensor technology

Intrusion and perimeter detection are essential for homeland security (such as border patrol), autonomous military RECON scouting, or securing a forward bivouac area. But the trouble with many sensors is they are either power hungry, not easily networked, or both. GreenPeak Technologies claims to have solved these problems – and more – with their Lime CM-08 module. The tiny 5 cm^2 (< 1 square inch) device functions as a stand-alone communications system with transceiver, antenna, and low-power mesh network software onboard.

The wireless transceiver and sensor interface allow users to connect appropriate sensors such as photocells, vibration detectors, infrared, or other devices. But the unit also doesn't require an external battery, relying instead on external solar, electromagnetic, or piezo-electric transducers for power. The onboard software carefully adapts the available power to the device's consumption. Finally, built-in mesh technology enables designers to create extended wireless IEEE 802.15.4 open-standard, self-healing, and self-forming low-cost networks based upon the ZigBee Alliance. Future versions hope to shrink the CM-08 module down to chip size.

GreenPeak Technologies
www.greenpeak.com
RSC# 36155

Editor's Choice Products

Low-cost "applique-like" military radio-based LAN

Well, things will be "all better" when JTRS is widely deployed. Joint service radios will interoperate, there'll be more bandwidth, and IP-based networks will rule the battlefield. But until then … the Sealevel Systems ACC-188 USB synchronous interface adapter allows a USB-equipped laptop (aren't they all?) to interface with a variety of legacy military radios. Boasting high throughput, the adapter allows war fighters to transmit and receive data such as GPS maps, images, coordinates, and even IM-type communications. Handy for the soldier updating his MySpace page.

The adapter is compatible with the following radios: Harris PRC-117 and PRC-150, Motorola LST-5, Raytheon PSC-5D and ARC-231, Rockwell Collins ARC-210, and Thales PRC-148. Additionally, the adapter can be used by most digital radios that have a synchronous serial port. Sealevel's included PDA-184 software product provides a GUI to manage the data transfer, protocols, and interface with the appropriate radio at the other end of the cable. We witnessed this product at the recent AFCEA conference in San Diego, and its simple elegance looks very compelling. [Full disclosure: Sealevel provided editors with a promotional gift as part of the product launch.]

Sealevel Systems • www.sealevel.com • RSC# 36154

TTP IP eschews ASIC for FPGA

Despite the acronym soup, the Time-Triggered Protocol specified by DO-254 and DO-178B Level A safety-critical systems no longer requires an ASIC to run. Instead, TTTech Computertechnik is making available its TTP controller IP (Intellectual Property), which can be synthesized into Altera Cyclone II or III FPGAs. The significance is not only the elimination of an ASIC in-system, but adding the protocol to a low-cost FPGA leaves additional gates free to replace other in-system functions.

Altera's Cyclone FPGAs can operate over -40 °C to +125 °C ($T_{junction}$), making them an ideal solution for extended temperature civilian and military applications. In fact, TTTech says the TTP will be deployed in the Boeing 787 Dreamliner and Airbus A380, as well as being used in the Lockheed Martin F-16. The TTP controller IP comes as a synthesizable netlist for Altera's Cyclone FPGAs, or even in Altera's HardCopy II structured ASICs.

TTTech Computertechnik
www.tttech.com
RSC# 36157

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Designing a battery charger for tactical operations

By Jeffrey VanZwol

When designing a charger for today's challenging military applications, a thorough understanding of battery capabilities and charger architectures, including those with dedicated charger ICs and microcontroller control, is necessary. Jeffrey provides an overview of these important features and the alterative charger architectures that can provide them.

An increase in military spending has provided a moderate boost for manufacturers of ruggedized or mil-spec battery packs. With the recent modernization of the military armament, soldiers are becoming more reliant on mobile power sources. The Land Warrior program provides a soldier system that improves situational awareness and communications for soldiers by connecting them via a wireless network and equipping them with head-mounted displays, computers, and sensors.

This next generation of mobile equipment carried by the "smart soldier" includes several pounds of battery packs. The current estimate is a soldier carries approximately 20 pounds of batteries. One of the objectives of the Land Warrior program is to consolidate multiple battery packs, powering numerous discrete devices down to a few common battery packs. In addition, many government and military procurement groups are leaning more toward rechargeable battery chemistries, driven by recent green initiatives and the total ownership cost of disposable batteries. As the percentage of disposable batteries grows, chargers for military batteries become more important to the survival and success of our military operations. Accordingly, battery capabilities and architectures are key considerations when designing battery chargers for modern military applications.

Current battery capabilities

Before a charger can be architected, one must consider and understand the battery chemistry and characteristics affiliated with the battery pack. Portable rechargeable cell chemistries include Alkaline, Nickel Cadmium (Ni-Cad), Nickel Metal Hydride (NiMH), and Lithium Ion (Li-ion). As presented in Figure 1, Li-ion provides the highest energy/density for portable or mobile applications. Lithium primary cells (called *primary* due to the one-time, disposable use model) are disposable and designed for single-use applications.

Battery technology has kept pace as portable military devices have become more

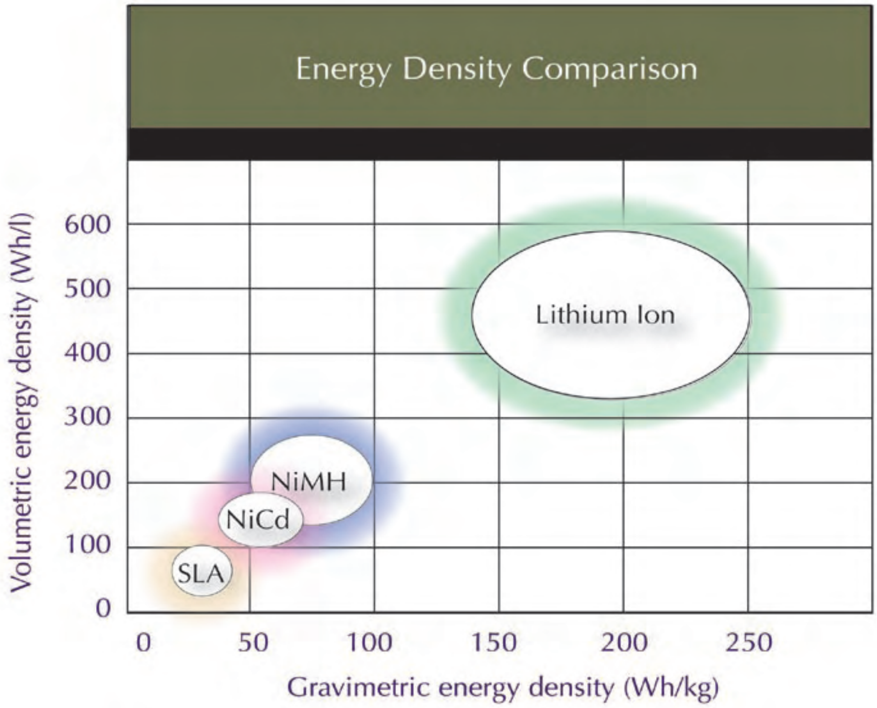

Figure 1

sophisticated and demanding. Today, most military OEMs are turning to smart Li-ion and Lithium Polymer (Li-polymer) battery pack solutions that have embedded intelligence to monitor their own state-of-charge and communicate via serial buses to the portable device. These chemistries offer the highest energy densities currently available and, in the case of Li-ion, a very competitive cost-per-watt-hour for their weight. With operating voltages ranging from 3.6 V to 3.8 V, only one rechargeable lithium chemistry cell is required for a 3 V operating system. In contrast, yesterday's nickel-based technology, which operated at 1.2 V, required three batteries for a 3 V operating system. Although NiMH systems can be configured with up to 10 cells in series to increase voltage, resulting in a maximum aggregate voltage of 12.5 V, Li-ion battery systems can be configured with up to 7 cells in series to increase voltage. This results in a maximum aggregate voltage of 25.2 V.

Multiple architectures for battery chargers

Demands on battery technology have required the use of more reactive materials; therefore, active safety circuits are required to ensure that certain battery chemistries are kept in a stable condition during charge and discharge. Even in less rugged environments, we have witnessed numerous battery failures in the past year that have prompted battery recalls from such vendors as Sony and Matsushita (Panasonic). With careful charger and

- Dual PMC/XMC Sites
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Targeting high-performance I/O and processing applications, the Model 4207 delivers an on-time solution for your real-time application using the latest high-speed serial interfaces.

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battery pack design, incidents involving battery rupture or explosion are very rare. However, it should be recognized that under certain charging conditions more likely in battlefield conditions (such as extreme temperatures or punctured batteries), the battery pack integrity can be breached and subsequently expose the user to harmful chemicals or even flames.

Designing battery chargers or docking stations has its own unique set of electrical challenges. One of the first considerations in designing chargers is the tradeoff between a dedicated charge control Integrated Circuit (IC) versus a microcontroller-based charging architecture.

Charging systems for military batteries typically have additional features over consumer chargers. An example of a military battery and charging bay is presented in Figure 2. Since military batteries support mission-critical applications, more intelligence is required to provide users with accurate state-of-charge information and expected battery performance. Examples of these features include: charging at high (more than 60 °C) or low (below -20 °C) temperatures, fast charging, state-of-charge indication on the charger (via LED or LCD), and monitoring and limiting the number of charge/discharge cycles for each battery.

Architectures with dedicated charger ICs

Dedicated charger ICs are embedded in cell phones, portable digital music players, portable DVD players, PDAs, and many other high-volume consumer products. They are particularly popular for low-power devices that are powered by a single cell Li-ion battery. Almost without exception, one will find an available charge controller that comes fairly close to meeting the fundamental design requirements of a consumer application.

Charging circuits for single cell and 2 cells in series batteries (referred to as 2S) is less complex, and many off-the-shelf charger ICs exist for these configurations. However, when one moves to 3S and 4S military Li-ion packs with higher voltages, there are noticeably fewer controller components available and the implementation becomes more complex, as more overhead parts are required in the charge control circuit.

Figure 2

Additionally, low-power alternatives (for example, charge currents of less than 2 A) permit the use of some very elegant dedicated charge ICs that contain power MOSFETs and the digital charger logic array on the same die. Lastly, a design that contains fewer parts has the potential for fewer manufacturing defects and higher MTBF.

However, the challenge with dedicated charging ICs is the minimal features for any given part and the subsequent inflexibility. Even with all the choices of components, finding one component that meets all of a product's requirements is not easy. This includes basic charge features such as waking up over-discharged Li-ion packs, precharging deeply discharged packs, supporting multiple charge termination thresholds for Li-ion batteries, and driving configurable LEDs for charge status indication. Support for advanced functions is more rare; these functions include battery drain/recharge, multi-bay charging with power management, and communicating accurate state-of-charge data with different variations of battery fuel gauge ICs.

Architectures with microcontroller control

An alternate approach introduced by charger manufacturers is a microcontroller architecture with software-controlled charging. Typically, every feature available in a dedicated charger IC can be implemented with a typical low-cost microcontroller. Many features offered via the microcontroller do not require additional hardware with a recurring part cost. Numerous communications protocols (SMBus, I^{2}C, HDQ) are supported with microcontrollers, and the firmware can be tailored to almost any implementation of a battery fuel gauge. One microcontroller can be multiplexed to control more than one charge bay. This is dependent on the number of I/O pins and PWM controllers driven or supported by the microcontroller, but generally three or four bays can be managed with one microcontroller. For multibay chargers, this can result in significant cost savings over step-and-repeat implementations of a dedicated charge IC. Finally, microcontrollers with flash memory can also support field upgradeability for changing battery chemistries, supporting new styles of battery packs, or adding additional features after initial release.

In addition to the aforementioned features, other examples of custom, differentiated charging features enabled by microcontrollers include:

- ***High temperature charging –*** Microcontrollers can vary the charge current to minimize temperature rise when the ambient temperature is already high.
- ***User notification through LED or LCD –*** Any color and pattern can be implemented with LEDs. State-of-charge indication is easily and inexpensively conveyed to users with a four- or five-segment LED or displayed on an LCD. Although most customers choose multicolor LEDs, the LEDs can be flashed or combined to indicate various charge states and error conditions.

> "One microcontroller can be multiplexed to control more than one charge bay … For multibay chargers, this can result in significant cost savings over step-and-repeat implementations of a dedicated charge IC."

- ***Gas gauge management and recalibration –*** Gas gauges can drift over time, and report inaccurate state-of-charge information. Microcontrollers can compare actual state-of-charge status (determined by progress in CC-CV charge cycle) to state-of-charge data (provided through the communications bus to battery).
- ***Wake up battery in sleep mode –*** Li-ion batteries will go into sleep mode if they are forced into an under-voltage condition. A microcontroller can check battery voltage, and if under voltage, can properly recover an over-discharged battery by applying a zero-voltage charge current.
- ***Limit the number of cycles for a pack –*** Military OEMs may wish to limit a battery's number of charge/discharge cycles so an overstressed battery does not go into the field. Once a battery exceeds a predetermined limit, the charger can refuse to charge the pack or alert the user.

Functionality and complexity drive architecture decision

As one considers which type of internal charger architecture to implement when designing a battery charger, one will conclude that dedicated charger ICs are best suited for fixed function, smaller, battery packs with stable temperature environments. When the battery pack configurations or charging environments expand beyond these optimal conditions, microcontroller architectures allow battery chargers to maximize operational readiness and battery performance, ensuring a refreshed battery provides maximum power and runtime when it is deployed in a harsh field environment. Vendors such as Micro Power are stepping up to the plate, providing a wealth of consulting, design, and manufacturing experience with battery chargers for use in rugged environments.

Jeffrey VanZwol *is a senior marketing executive with more than 18 years of experience in all aspects of technical marketing, including product management, product marketing, marketing communications, and partner management. He has extensive presentation experience on a wide variety of technical topics and has presented at conferences such as Advancements in Battery Technology and Power Management conference, Power Systems World, and the Military Technology Conference. Jeffrey earned a Bachelor of Science degree in Computer Science from Saint Francis Xavier University and a Master's degree of Business Administration from McGill University. He can be contacted at jvanzwol@micro-power.com.*

Micro Power Electronics
503-693-7600
www.micro-power.com

New Products

By Sharon Schnakenburg

MIL-STD-1553 PCI INTERFACE CARD

Alta Data Technologies
Website: www.altadt.com
Model: PCI-1553 **RSC No:** 35957

A 1-4 dual redundant channel MIL-STD-1553 PCI interface card that provides advanced features for communications (such as JTIDs, Link-16, SADL), testing, and simulation • 1 MB high-speed QDR RAM for fast host access • Signal capture on first channel • Eight-bit A/D standard on all cards • Signal generator • Advanced buffering for all modes • Dual function BC/Mon or mRT/Mon, or full function BC/mRT/Mon • Full legalization per MIL-STD-1553 to word count level and all mode codes • Multi-layer API for RTOS, Linux ANSI C support to Windows Linux ANSI C • LabVIEW native support with .Net assembly • Supports AltaView and AltaRTVal software packages to extend test, simulation, and validation

RUGGED ATR ENCLOSURES

Carlo Gavazzi Computing Solutions
Website: www.gavazzi-computing.com
Model: 715 Series **RSC No:** 36019

Air-cooled rugged ATR enclosures • Engineered for maximum protection of COTS cards deployed in caustic environments • Designed to withstand extremes in temperature, vibration, humidity, and contaminants • Recirculating air cooling system provides a contaminant-free environment for COTS convection-cooled cards • While functioning as a typical conduction-cooled system on the outside, the cooling system for the 715 Series uses a recirculating fan on the inside to transfer circuit card heat energy to the conducting walls • Conducting walls are engineered thermal cores providing maximum heat transfer to the system's exterior surfaces • Features a rugged, brazed aluminum frame construction • Available with scalable power options • Can be configured to custom form factor requirements for a variety of airborne applications

LCD ANALOG RESISTIVE TOUCH SCREEN

Core Systems
Website: www.coresystemsusa.com
Model: MP21-STN NEMA 4X **RSC No:** 35951

A 21" active-matrix LCD analog resistive touch screen with 1,600 X 1,200 picture quality • High brightness, ultra-high contrast (900:1) • NEMA 4 / 4X / 12 • Black powder coated carbon steel or stainless steel faceplate • Only 2.2" deep (behind panel) • Analog USB and serial resistive touch screen • VGA, Digital Video (DVI), S-Video, and composite inputs • Thin-Film Transistor (TFT) active matrix liquid crystal • Size - 21.3" diagonal • Native resolution - UXGA (1,600 x 1,200) • Min. resolution - VGA (640 x 480) • Pixel pitch - 0.27mm x 0.27mm • Brightness - (white) 300 nits (cd/m2), typical • Input connector - HD-15, DVI digital, S-Video, composite RCA • Input signal format - Analog RGB signals, DVI Analog/Digital, CVBS, S-Video • Response rate (typical) - 8 ms typical • Panel rating - NEMA 4/12 or NEMA 4/4X/12 • Shock - 30 *g* (1/2 sine, 11 msec) • Vibration 0.006" p-p 15-57 Hz, 1.0 *g* 57-640 Hz sine • Temperature - 0 to 50 °C

PC/104-*PLUS* 1553 CARD

Data Device Corp. (DDC)
Website: www.ddc-web.com
Model: BU-65578Cx **RSC No:** 35574

A PC/104-*Plus* 1553 card ideal for fitting 1553 into space-constrained applications • Based upon DDC's own Extended Enhanced Mini-ACE (E2MA) 1553 chipset • Up to four dual-redundant 1553 channels • 2 MB of parity memory per channel • BIT, robust transmissions, and data transfer are assured • Five user-programmable digital I/O channels • IRIG-B time code input • External time-tag clock input • 48-bit/1 microsecond time stamp capability • -40 °C to +85 °C version available

RUGGEDIZED INDUCTORS

Datatronics Distribution
Website: www.datatronics.com
Model: DR370 Inductor **RSC No:** 35950

Inductors that combine high performance and a wide inductance range in challenging EMI operating environments • Rugged packaging • RoHS-compliant lead material • Inductance range from a low level of 0.31 µH to an upper range of 2.2 µH • DCR is specified from 0.75 to 4.0 mOhms maximum over a maximum current rating from 20 to 42 A • Compatible with temperatures ranging from -55 °C to +125 °C • Custom-designed DR370 inductors can be specified to meet unique circuit requirements

PC/104 SBC

Diamond Systems Corporation
Website: www.diamondsystems.com
Model: ATHM500-256A **RSC No:** 35704

Part of the Athena II family of PC/104 expandable SBCs • 500-800 MHz wide temperature VIA Mark CPU with integrated data acquisition • Low-power fanless operation • 256 MB memory soldered on board • 10/100 Mbps Ethernet • S3 Savage 4 chipset with advanced 3D/2D video • Four RS-232 serial ports • Operating temperature range: -40 °C to +85 °C

CompactPCI Express SBC

Dynatem, Inc.
Website: www.dynatem.com
Model: EPD
RSC No: 35955

Core Duo based 6U CompactPCI Express single board computer • 6U CompactPCI Express form factor per PICMG EXP.0 system slot specification • PICMG 2.16 compatible • Pentium Core Duo processor @

Continued on page 57

High-Speed USB Solution to Data-Enable Tactical Radios

Warfighters can transmit/ receive GPS maps, images, coordinates, and IM communications.

- USB synchronous radio adapter cable
- High-speed data throughput
- Interoperable (Send/receive data with different radio models and brands)
- Hot swappable

Available with a variety of radio connection options that make it compatible with the most prevalent brands and models:

Harris PRC-117	Raytheon ARC-231
Harris PRC-150	Raytheon PSC-5D
Thales PRC-148	Motorola LST-5
Rockwell Collins ARC-210	

Call and ask about your specific models.

Sealevel Systems has the high-speed solution to data-enable tactical radios: a USB synchronous radio adapter cable and free DISA PDA-184 software. Connect the plug-and-play cable to your computer or handheld device via USB[1] and to your tactical radio. It's that quick and easy for warfighters to enhance their critical high-speed data communications in the battlefield.

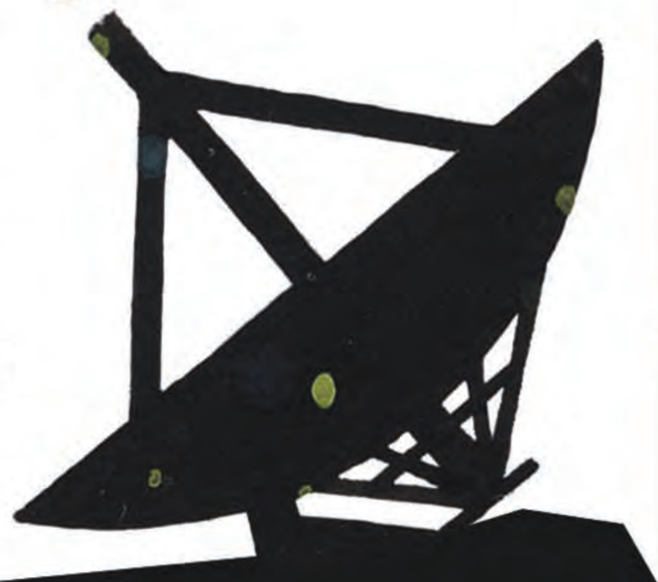
The PDA-184 software is government-developed, government-owned by DISA and is available from Sealevel as part of this total solution.[2] Features include:

- Implements MIL-STD-188-184 Data Waveform
- Easy-to-use Java-based GUI
- Runs in Microsoft Windows XP or 2000

Contact us at **864.843.4343** or **sales@sealevel.com**

[1]Also available with PCMCIA connection.

[1]Able Communications Technology Corporation, under contract to DISA, provides engineering and software development expertise for the PDA-184 Software in addition to supporting the revision of MIL-STD-188-184 along with other UHF SATCOM MIL Standards.



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Committed to American made.
Honored to have 20+ years serving the military.

SEALEVEL

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Continued from page 54

1.66 GHz • Supports two PMC sites, one of which optionally supports XMC modules • E7520 chipset for PCIe support and high memory bandwidth • Single-slot, 4HP design with option for additional one-slot storage module

MINI-ITX SBC

iBase Technology
Website: www.ibase-i.com.tw
Model: MI935 **RSC No:** 35572

A Mini-ITX form factor SBC • Supports Intel's Core 2 Quad/Core 2 Duo/Celeron 400 sequence processors (Conroe-L) and Intel's latest Q35 Express chipset with a full 1,333 MHz FSB • Notebook computer-sized dimensions of 6.7" x 6.7" (170 x 170 mm) • Two DDR2 DIMM slots • Can support up to 4 GB of DRAM • 10/100BASE-T Ethernet port, integrated VGA, 8x USB 2.0, 2x SATA II, 1x eSATA, and 2x COM ports • Optional I/O includes a 1x PCIe GbE, a second VGA via PCIe (x16), and four more COM ports • Suitable choice for full-featured but small-sized PC-based military systems

DDR3 CLOCK REFERENCE BOARD

Inphi Corporation
Website: www.inphi-corp.com
Model: DDR3 CRB **RSC No:** 35795

A DDR3 Clock Reference Board (CRB) designed specifically for high-performance RDIMM testing • Performs beyond JEDEC DDR3-1600 specifications, achieving clock speeds of 800 MHz • Provides a comprehensive validation tool for DDR3 register/PLLs • A fully programmable pattern buffer delivers more accurate test results by allowing customers to create test conditions specific to their applications rather than relying on limiting preprogrammed patterns • Design teams can adjust timing for control or address lines in 10 ps steps, allowing them to precisely resolve limits on their designs and providing more reliable test results • Uses the open source Python GUI • External clock reference • Input signals are buffered to provide clean reference signals, margin, and voltage timing • Customers can perform a more complete test that discovers bugs earlier in the design cycle simply by adjusting the Vdd and/or Vref power

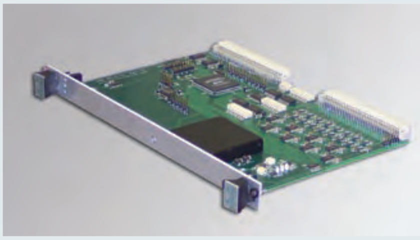
RUGGED 3U RAID SYSTEM

Phoenix International
Website: www.phenxint.com
Model: RPC12 **RSC No:** 35575

A SAS/SATA II 3U RAID system providing ruggedness, reliability, and portability • Up to 12 HDDs in carriers • Capable of withstanding 60 *g* shock at 2 ms • Operates over 5 °C to 60 °C and up to 40,000 feet with sealed HDDs • Accommodates RAID 0, 1, 3, 5, 10, 50, NRAID, and JBOD, along with dual hot-swap PSUs and cooling fans • Host interfaces include 2 or 4 Gbps Fibre Channel, serial attached SCSI, or iSCSI • Input voltage ranges from 40 to 440 Hz and from 90 to 240 VAC • Interfaces to Windows, Linux, and UNIX • Includes a management GUI and failover software

6U VME ANALOG OUTPUT CARD

Precision Analog Systems (PAS)
Website: www.precisionanalog.com
Model: PAS 9915/AO **RSC No:** 35799



A VME analog output card • Provides 32, twelve-bit analog voltage output channels on a 6U VMEbus card • DAC resolution: 12 bits • VME Interface: A32, A24, A16; D32, D16 slave, no interrupts • Simultaneous update: Software or external sync updates DACs simultaneously • DAC power supply: Onboard ± 15 V DC-to-DC converter • Card power requirements: 5 V at 1.5 A, (typ) • Operating temperature range: 0 to 60 °C

RUGGED TABLET PC

Roper Mobile Technology
Website: www.ropermobile.com
Model: DUROS Rugged Tablet PC **RSC No:** 36020

A fourth-generation, Windows XP-based tablet PC • Sealed to IP-65 levels for dust and water ingress and manufactured to MIL-SPEC 810F • Built for "anywhere" use • Equipped with an 8.4" brilliant sunlight viewable, SVGA resistive touch screen • AMD Geode LX 800 processor or Intel Celeron M 1.0 GHz • Packs up to 1 GB memory and up to 120 GB storage (up to 64 GB solid-state drive) • Hot-swappable battery feature diminishes downtime and extends battery life • Equipped with integrated Wi-Fi, Bluetooth, GSM, GPRS, EDGE, UMTS, and optional built-in GPS for flexible communication options for extremely remote or harsh field applications

1U DUAL SERVER SUITE

Technology Advancement Group
Website: www.tag.com
Model: SV-1200 **RSC No:** 35693

A dual server suite in a 1U chassis • Two completely independent servers with their own power supply • Chassis specifications: Dimensions: 1.75" H x 19" W x 24" D; weight: 28 lbs • Specifications per server: Power supply: (1) Independent solid-state auto-switching power supply; processor: two Quad-Core Intel Xeon processors LV 5318; 5000P chipset/1333/1066/667 MHz; up to (2) 2" hard drives (SATA), expandable up to 1.2 TB total storage capacity; onboard ATI ES1000 w/16-bit memory

For more information

Enter the product's RSC# at
www.mil-embedded.com/rsc

Crosshairs Editorial

Recession-resistant tech

If you're working with one of these, the future looks brighter

By Chris A. Ciufo, Editor

With a recession on the way, or already here, some technologies stand a better chance of receiving funding or being purchased. Technology that can directly make a connection to an *end user benefit* is the secret here. With 2008 S&T funding reduced by an astounding 20.1 percent to $10.9 billion[1], the military science fair is over, kids, as only DARPA gets to play with the fun toys. Instead, the DoD prefers to buy only "right now" capabilities.

At the top of the list is anything that helps the U.S. prosecute the Global War On Terror (GWOT) while saving the lives of service personnel. Communications gear, crypto and secure software are also hot, as long as an end-user direct benefit can be made. Low power or devices that extend battery power are crucial. And any hardware or software platform that can build off of a legacy system's software or hardware puts you several steps ahead of the game and your competition. That edge might just get you funding.

One in a crop of interesting new doodads is Ambric's *Massively Parallel Processor Array,* being targeted at defense and security applications. It's never a good time to be a processor company – much less start one – but these folks have been at it since 2003 and have spent only $21 million of Series A funding. Their tiny burn rate has given them big credibility with the DoD, as has the CPU's amazing performance. Designed as a stream processor at the front end behind a sensor, the 1 TeraOPS, 336-processor device maximizes MIPS/mW: Think of it as a Cray-on-a-chip. That means a lot less power in a much smaller space, putting to shame general purpose DSPs (5-20X over a TI C641x, they say), or FPGAs that require complex RTL coding.

As we went to press, Ambric was literally en route to present a paper about on-the-fly partial CPU reconfiguration – a particularly handy trick for data mining, cognitive radio, and myriad other military algorithms. DSPs can't do that, and Xilinx's FPGAs are only now sort-of talking about partial reconfigurability.

One of the ways Ambric might find its way quickly onto the battlefield is deployed in a VITA VPX chassis mounted in an MRAP for counter IED operations (more on IEDs in a moment). Itself a shining example of rapidly developed and deployed technology, the Mine Resistant Ambush Protected armored vehicles are being rushed to Iraq and Afghanistan to replace the woefully inadequate HWMMV. Some of those Hummers might also be finally equipped with VITA's now-available VPX technology, which is all about the I/O – *lots* of I/O.

Far as I can tell, Curtiss-Wright Controls Embedded Computing recently became the industry's very *first* COTS vendor to announce a VPX design win – for the Marines' Ground/Air Task Oriented Radar (G/ATOR). It's not in an MRAP, it's in a Hummer. And it is an FPGA-based DSP board integral to the Active Electronically Scanned Array (AESA) radar used for tracking air- and ground-based targets, as well as general air traffic control. Here too, CWCEC had the technology ready to go, and VPX was the ideal form factor for *quick field deploymen*t. The prime, Northrop-Grumman, awarded CWCEC $4.3 million for their efforts. Kudos.

And with technology budgets thinner now than at any time during the Bush Administration (O&M for two fronts is taking the lion's share), extending the life of anything – particularly software – is key. No one has the time or money to write code from scratch if modules can be reused. I call this *Legacy Software Migration,* and it will form the basis of a new, regular column in this magazine starting in May. But in this issue, contained in our "RTOS updates and trends" feature on page 16, the most common theme I found from our industry survey is how easy it really is to migrate forward software and hardware.

It's all about reuse, folks. For instance, if you believe Ada is so 1990, then either Aonix or DDC-I can move you into safety-critical Java. Or MapuSoft can "easily" migrate you from one hardware platform to another while preserving legacy code. As well, Impulse Accelerated Technologies – from which we'll hear in a future issue – has a slick way of abstracting an obsolete PowerPC chip into an FPGA. Besides that, Quantum3D has a software-based GPU called IGL178 that is obsolescence-resistant. Common theme with all of these: saving time and money and getting a useable system to the field, double-time.

And no one knows more about double-time than the Joint IED Defeat Organization (JIEDDO). These folks are all about rapidly deployed tech rushed to the front lines to counter IEDs and save lives. At the well-attended recent *Military and Aerospace Electronics Forum,* JIEDDO Deputy Director Dr. Robin Keesee talked about whittling 1,335 proposals down to 17 major funded initiatives in an astounding 68 days. Technology to save lives can be fielded, he said – proposal to deployment – in a mere *six months!* Compare that to JTRS, which is going on maybe eight years.

These represent the kinds of technologies that are getting funding as a recession looms. Not every VPX board, FPGA SDR, or C cross-compiler will see such a short time-to-money. But making sure *your* technology or *your* program has a direct end-user benefit will dramatically enhance the chance of funding or program success. Don't let DARPA have all the fun.

Chris A. Ciufo
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[1]The first drop-off in seven years, according to the American Association for the Advancement of Science, a nonprofit group. See www.aaas.org/spp/rd/08pch5.htm for details.

MIL/COTS DIGEST
The Defense Electronic Product Source
Mar/Apr 2008

In This Issue

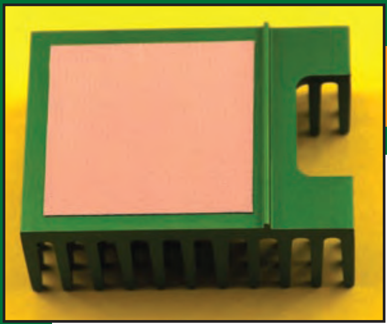
A "boxed set" – including chassis, backplanes, and mechanicals ...

As promised, here is the first of our now-quarterly *MIL/COTS DIGEST (MCD)* supplements in 2008. Why tickle your mailbox with MCD's signature green and gold layout twice as many times this year than last? Because of an overwhelmingly positive response from *Military Embedded Systems* readers ... and of course, a little thing called "technology innovation." Indeed, our challenge as editors to keep up with the latest-and-greatest tech trends to hit the market is never-ending, but nevertheless (and needless to say), something we truly enjoy.

This year, you'll find something a little bit different in every *MCD* supplement as each will be themed from now on, as opposed to our previous "potpourri" approach. The edition you're holding in your hands focuses on chassis, connectors, and backplanes galore. In the July/August edition, though, you'll find *MCD's* pages filled with VME-related products, and in September a plethora of DSP/SDR products. And last, but definitely not least, our November/December issue will center on power conversion, batteries, and power management.

Until then, I'm once again sharing my "hand-selected" favorites within this edition's glossy pages. Though these products might be considered less glitzy than others such as glamorous SBCs or high-end graphics processors, the connectivity products you will find may just be at or near the backbone (or is that the "backplane") of your next project.

Chris Ciufo, Editor
cciufo@opensystems-publishing.com

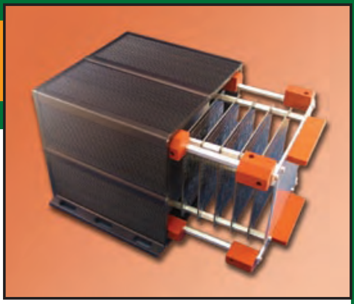


Thermally conductive silicone film

Keratherm 86/82 is a thermally conductive, electrically isolating silicone film with a reinforcing fiberglass layer for tear and cut-through resistance. The silicone provides excellent wetting properties for filling interface surfaces; meanwhile, a high-tensile strength Thermal Interface Material (TIM) improves heat transfer from ICs and other components to their heat sinks and provides durability for installation and long-term use. Thermal impedance is 0.05 W/m-K, and thermal conductivity is 6.5 W/m-K. With its fiberglass layer, the 86/82 has a tensile strength of 20 N/mm^2. Its material meets UL 94V-0 flame class requirements, and its continuous use temperature range is -40 °C to +200 °C. Standard material thickness is 0.250 mm (9.8 mil), and pads are also available in 0.300, 0.400, and 0.500 mm thicknesses (11.8, 15.7, and 19.6 mil).

www.mhw-intl.com **MH&W INTERNATIONAL**

PCI-104, PC/104-*Plus*, PC/104 rugged chassis



Dynamic Engineering's PC104p-Chassis is a rugged chassis for PCI-104, PC/104, and PC/104-*Plus* systems with built-in heat sink, mounting flange, and watertight design. One to 11 cards plus custom are available, and 5-11 slots are standard with the 5-slot model covering 1-5 cards installed. The chassis' rugged design has machined end plates, built-in gaskets, and an internal shock-mounted card cage. The extruded design allows for multiple lengths, and a 1" x 3" chamber is found on each side for stack cabling. The PC104p-Chassis is customizable for user connectors and silk-screen requirements. Meanwhile, a built-in mounting flange with slotted mounting points adapts to a variety of system requirements and can be used for conductive cooling. A power supply (+12, -12, +5, +3.3, and -5) is available.

www.dyeng.com **DYNAMIC ENGINEERING**

Modular MicroTCA cabinet

The MicroTCA Cabinet by Optima Electronic Packaging Systems features a stacked arrangement of open card cages, fan trays, and heat exchangers. It also includes a 19" cabinet per ETSI 300-119-3, along with cable management and EMI shielding, liquid heat exchange capabilities, and closed air loop. The cabinet accommodates 10 MicroTCA card cages for single-width AdvancedMC modules and has a four-point latching system door, five heat exchangers, five fan trays, and a power supply tray.

www.optimaeps.com
OPTIMA ELECTRONIC PACKAGING SYSTEMS

ATR military chassis

The CM-ATR-x5 Series is a range of new-generation chassis that introduces the concept of Universal Military ATR enclosures capable of accommodating and freely intermixing all standard conduction- and air-cooled Eurocard formats. Each model includes four off-the-shelf cooling options: standard sealed – low-cost standard dry-air enclosure with inner fans for internal air recirculation; sealed with extended fins – self-dissipation sealed enclosures that incorporate internal air recirculation fans; flowthrough air-cooled – nonsealed chassis in which ambient air is directly forced over electronic modules using rear-mounted exhaust fans; and heat exchanger sidewalls – high-performance dry-air chassis incorporating air recirculation fans inside. All models feature slot-by-slot user-configured card cage to enable intermixing conduction-cooled IEEE-1101.2/ANSI-VITA 30.1 and air-cooled IEC-297/IEEE-1101.1 boards.

www.cmcomputer.com
CM COMPUTER

AdvancedMC load board

Elma Electronic's single-width, full-height AdvancedMC Load Board provides testing of power and cooling in MicroTCA systems. The device features IPMI support, is hot-swap pluggable, and handles configurable loads ranging from 0 to 70 W in seven steps. Commands are issued via the front-panel push button, and the load board has temperature sensors onboard.

www.elma.com
ELMA ELECTRONIC

Air-cooled rugged electronic enclosures

The 709 Series air-cooled rugged electronic enclosures for computer cards addresses the needs of harsh-environment applications such as shipboard and land-based military applications. The enclosures are configured for flexibility, accommodating up to 20 slots for VME64, VME64x, VXS, VPX, VXI, or CompactPCI cards from 8U to 15U high and 20.5" deep. Available in AC/DC or multiple-output power configurations of up to 2,000 W, the 709 Series cooling can also be configured in three ways: pressurized, evacuation, or combination push/pull. Featuring either overlapping bolted or welded construction, the EIA rack-mountable 709 Series is engineered to meet military specifications including MIL-STD-901, -810, -167, -704, and -461. The chassis can be outfitted with shock-isolated peripheral bays and configured to meet the highest EMI requirements.

www.gavazzi-computing.com **CARLO GAVAZZI COMPUTING SOLUTIONS**

19" modular PicoTCA chassis

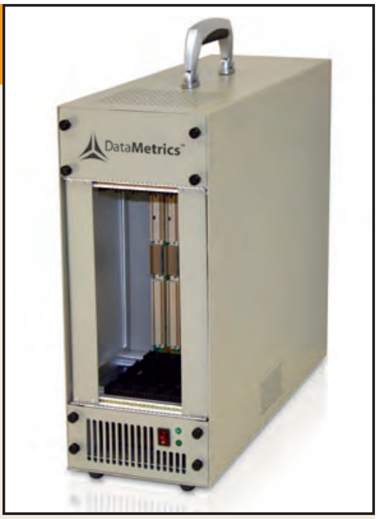
The PicoTCA Chassis is a modular 19" chassis in 2U design supporting up to 12 AdvancedMCs and an MCH in full-size and compact form factors. The unit complies with PICMG MicroTCA 0.R1.0 and AMC 0.R1.0 and is also NEBS compliant. The 482.6 mm x 254 mm rack-mount chassis includes two hot-swappable fan trays (push-pull) and an exchangeable air filter. The RoHS-compliant PicoTCA Chassis also includes AC/DC integrated JTAG connectors and supports up to 12.5 Gbps. A full range of faceplates and filler panels is available.

www.kaparel.com **KAPAREL CORPORATION**

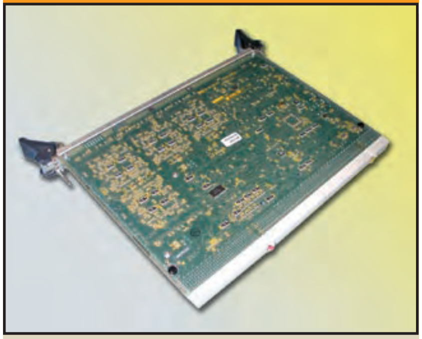
4U COTS mini-tower chassis

Datametrics Model 7004 is a COTS mini-tower chassis in a 4U form factor. It supports up to a seven-slot Eurocard backplane and is available in CompactPCI, VME64x, VITA-xx, or custom backplane configurations. A push-pull fan system provides aggressive cooling characteristics, and upper and lower fan trays come in an LRU design. The unit provides full access to all slots in 6U x 160 mm front subrack and all slots in 6U x 80 mm rear transition module subrack. Model 7004 has a front-mounted, illuminated power switch and rear-mounted circuit breaker. A 600 W power supply is standard, and an optional "Envirostat-2" chassis is available.

www.datametrics.com
DATAMETRICS



CompactPCI solder side covers

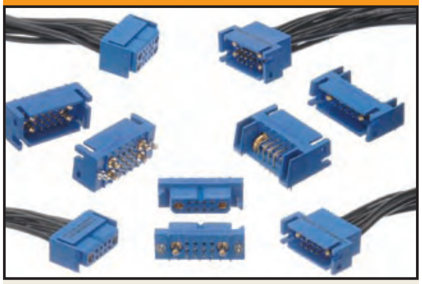


CompactPCI Solder Side Covers from 3-D Engineering attach to the backside of PCBs to safeguard components from damage during hot-swap insertion or extraction from a chassis. The low-cost, high-quality covers are washable and permanently antistatic, never needing replacement once installed. Solder Side Covers meet UL94-V0 requirements and feature a nominal thickness of .020". The barcode-scannable covers are washable and free of color. They provide surface resistivity of <1.0 x 109 (using EOS/ESD S11.11-1993 test method) and are compliant with NEBS standards. Solder Side Covers provide heat deflection of +61 °C.

www.3deng.com

3-D ENGINEERING CORP.

Mixed density connector

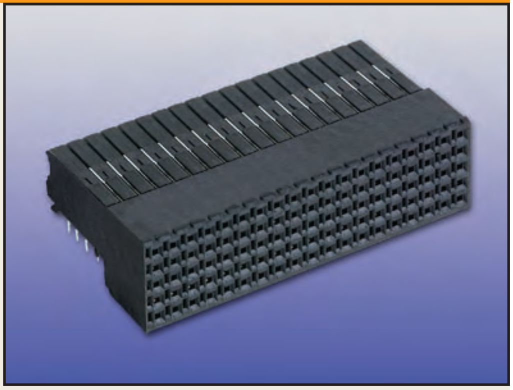


Positronic Industries' PCS Mixed Density connector combines size 8 power contacts and size 20 signal contacts in a single housing. The device conforms to UL requirements for 300 VAC applications, and size 8 power contacts have a resistance as low as 0.0003 ohms and can carry up to 85 A per UL 1977. The PCS Mixed Density connector is available with 2 power and 8 signal contacts, or 4 power and 10 signal contacts in solder, press-fit, and cable terminations. Other features include an integral locking system and blind mate capability.

www.connectpositronic.com

POSITRONIC INDUSTRIES

High-speed, hard-metric connector



The 3M MetPak HSHM B19 connector supports speeds of up to 5.0 Gbps per differential pair while maintaining full pin-to-pin compatibility on the backplane with VME64x, P0 VITA 31, and P3 PICMG 2.16 connectors. The MetPak HSHM B19 is designed to meet the industry standard 2 mm hard metric format in accordance with IEC-61076-4-101. The device uses virtual coaxial shielding technology to provide maximum performance with minimal cross-talk and skew. The connector also enables fully compatible designs with fast serial links running up to 5.0 Gbps per differential pair, permitting PCI Express and RapidIO to be run on existing backplanes without an expensive or disruptive backplane upgrade. Additionally, the device enables the extension of the life of, and preserves the investment in, existing VME and CompactPCI systems.

www.3M.com/electronics **3M ELECTRONIC SOLUTIONS DIVISION**

19" rugged rack-mount VME/VXS chassis

The MC3000 VME/VXS from MCH Systems, Inc. is a 19" rugged rack-mount VME/VXS chassis with fault-tolerant fans and a redundant 1,000 W power supply system. Designed for shipboard, airborne, and ground mobile military applications, the MC3000 is designed per IEEE 1101.10/11. Rugged aluminum card cages include front: 6U 160 mm; rear: 6U 80 mm. Hybrid backplanes include VME, VXS modules, and hot-swap power supplies. Meanwhile, a fault-tolerant, demand-driven cooling system provides 400 lfm across components with front air intake and rear exhaust. Additionally, front-panel maintenance for removing modules, power supplies, and fan tray is available, and front-panel LEDS indicate failing modules. The MCS3000 system monitor features RS-232 output and discrete inputs, and the device operates from -20 °C to +60 °C.

www.mchsys.com **MCH SYSTEMS, INC.**

8U powered crate series

The VME8100 is a VME (64/64x) 8U (6+2) powered crate series with 21 slots for 6U x 160 mm VME modules. The device accommodates pluggable power supplies with different configurations up to 2,500 W and is available with a VME64/VME64x compliant monolithic backplane. The VME8100 features a pluggable 2U fan unit, along with short-circuit protection and over/undervoltage and overtemperature protection. The power crate interfaces via CANbus, Ethernet, USB, and RS-232 interfaces for remote monitoring and control. The CBLT-compliant VME8100 is also SBC controlled with a graphic OLED display.

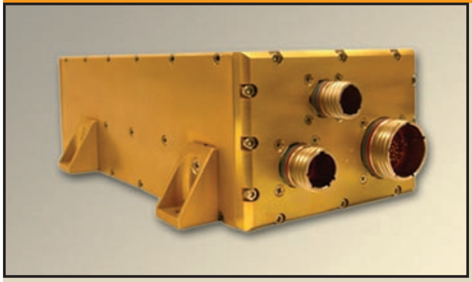
www.caentechnologies.com **CAEN TECHNOLOGIES, INC.**

Liquid-cooled ATR chassis

Elma Electronic's modular, liquid-cooled Air Transport Rack (ATR) chassis can be configured in various sizes and configurations without starting from scratch. It can also fit up to ten 6U x 160 mm slots in a 1 ATR short size. Designed to ARINC 404A, the chassis accepts conduction-cooled modules in various architectures such as VME64x, CompactPCI, VXS, VPX, and more. Independent dual liquid-cooled sidewalls dissipate in excess of 100 W per slot, and various cooling fluids can be used including glycol, kerosene, PAO, and salt water. With a proven high-integrity frame construction, the unit is highly ruggedized and meets MIL-STD-810E, -461D, and -704E.

www.elma.com **ELMA ELECTRONIC**

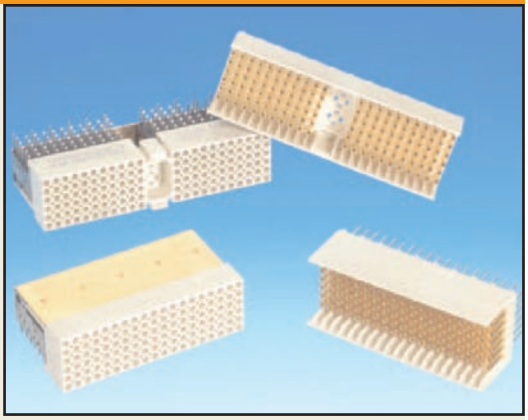
Environmentally sealed, EMI/RFI protected chassis



Aitech's E192 is an environmentally sealed, lightweight, compact, and EMI/RFI protected chassis. It is well suited to mobile military applications such as glass cockpit avionics computers, mission computers, weapons control, and data handling/data management subsystems. It accommodates six standard ANSI/IEEE1101.2 conduction-cooled, VME64x VMEbus boards with an 0.8" pitch as well as commercial VMEbus boards. The VMEbus backplane is offered either in a user-customizable wire wrap configuration, or prewired per customer specification. The conduction-cooled VMEbus boards are sealed in an EMI/EMC proof Faraday cage, and the chassis is externally fan/forced air-cooled. Dissipating over 215 W at 55 °C (131 °F), the chassis accommodates a wide variety of standard MIL-STD-704A and -704D vehicle power from 28 Vdc to 115 VAC and 40 Hz to 400 Hz input voltages.

www.rugged.com **AITECH DEFENSE SYSTEMS**

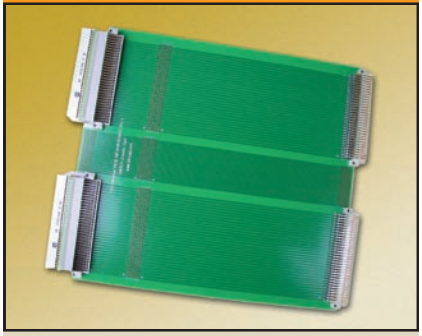
2 mm CompactPCI connectors



Hypertronics 2 mm connectors are tested to military standards and deliver high performance in a ruggedized CompactPCI format for mission-critical applications. They feature a standard 2 mm footprint interchangeable with CompactPCI COTS systems. The devices' Hypertac contacts provide high reliability and immunity to shock and vibration fretting. In addition, a keying feature ensures proper mating. The connectors' high-temp LCP insulator meets NASA outgaussing requirements, and a shield prevents EMI/RFI.

www.hypertronics.com **HYPERTRONICS**

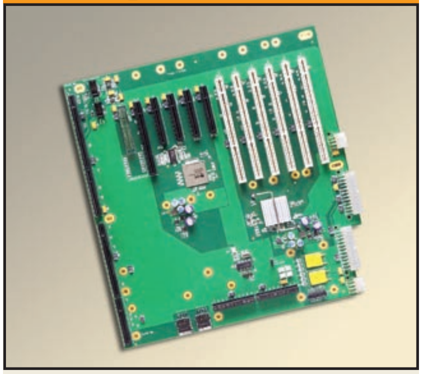
VME64x Extender Card



The VME-8198-EXTM-LF extender card supports 160-pin connectors as standard, along with J/P0 connectors and additional backplane-style connectors as optional. The extender card also features test points for monitoring signals and lead-free assembly. The six-layer, 6U VME64x device is designed for five-row, J/P 1 and 2 connectors and P/J0 connectors. It achieves straight pin-to-pin connections; additionally, standard build includes male right and female 160-pin connectors.

www.twinind.com
TWIN INDUSTRIES, INC.

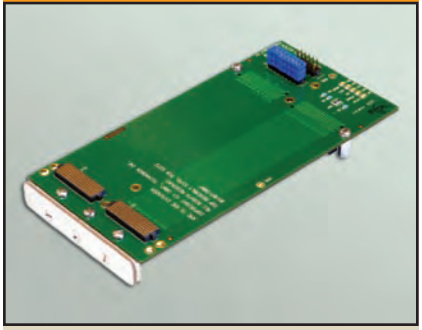
Server-class backplane



The S6615 is a server-class backplane that supports five PCI Express, four 64-bit/66 MHz PCI-X/PCI, and two 64-bit/100 MHz PCI-X/PCI option card slots. Graphics-class backplane configuration maximizes PCI Express bandwidth for graphics applications. The backplane includes one x16 PCI Express slot, four x8 PCI Express slots, two PCI-X 64-bit/100 MHz slots, four PCI-X 64-bit/66 MHz slots, and four USB 2.0 backplane I/O connections. The SS6615 also includes one 10/100/1000BASE-T backplane Ethernet port.

www.chassis-plans.com
CHASSIS PLANS

XMC-to-XMC extender



The Technobox, Inc. model 5270 is an XMC-to-XMC extender that can be installed on an XMC site of a VME, CompactPCI, or other carrier board to allow the extension of an XMC module for test access. In addition to providing extension, the unit also elevates (by approximately 11 mm) the mounted XMC. The P15 to J15 traces are routed for PCI Express signaling. P16 signals, however, are routed in a 1:1 fashion with the differential signals routed with 100 ohms. (Differential pairs are impedence controlled.) The RoHS-compliant 5270 features a pair of JTAG headers – JP1 and JP2. The first is intended to accept connection of an Altera programmer, and P2 allows a user to access the JTAG and I2C signals for the carrier and mounted XMC.

www.technobox.com

TECHNOBOX, INC.

1U rack server chassis

The 1U Rack Server A270 is a compact chassis built for industrial applications in various sizes, including 1U. The unit includes an AMD Athlon 64 x2/Athlon 64, 35 W CPU. The A270 supports 1U power supply up to 250 W and has one 3.5" disk capacity. The chassis also features two USB connectors on the front panel and a 4 cm cooling fan.

www.joergerinc.com

JOERGER ENTERPRISES, INC.

Male-female stacking spacers

Stacking Spacers from RAF Electronic Hardware are male-female stacking spacers in round and hexagonal profiles in nylon and aluminum. They are precision manufactured for demanding PC/104 and PC/104-*Plus* embedded applications. With RAF Stacking Spacers, circuit boards are spaced exactly 0.6" apart to build structurally secure module stacks. The stand-alone stacks can be used like ultra-compact bus boards, but without the need for backplanes or bird cages. Additionally, the spacers help overcome space limitations that may occur during the installation of PC/104 and PC/104-*Plus* embedded bus drives. RAF male-female Stacking Spacers are 3/16" in diameter, have a 3/16" long 4-40 male thread on one end, accept a 4-40 thread screw on the other end, and have available mating screws and hex nuts in both nylon and aluminum materials.

www.rafhdwe.com **RAF ELECTRONIC HARDWARE**

ExpressCard cable adapter

The OSS-PCIe-HIB2-EC-x1 is a PCI Express (PCIe) x1 ExpressCard cable adapter enabling laptops to operate with high-speed expansion capabilities. The adapter provides cable connectivity from a laptop to devices such as desktop storage devices, video monitors, and add-in board expansion boxes via a PCIe x1 cable connector. (No additional drivers required.) The OSS-PCIe-HIB2-EC-x1 is used with SuperSwitch and ExpressNet to provide communication between laptop and PC. It comes in an ExpressCard 34 with connector extension and measures 1.34" x 4.83" (34 mm x 122.6 mm). Key features include a 2.5 Gbps serial PCI Express repeater/equalizer, LVPECL Spread Spectrum reference clock buffer outputs, and electrical isolation at the cable connector. The device supports up to 7-meter passive and 25-meter active cables based on the PCIe cable standard.

www.onestopsystems.com **ONE STOP SYSTEMS INC.**

3U MicroTCA shelf

The 11850-003 is a 3U x 19" rack-mountable MicroTCA shelf designed for maximum configuration flexibility. The backplane supports up to 10x single, full-size AdvancedMC slots, 2x MCHs, 2x PM slots, and 2x 12HP power modules. Active cooling is available via 2x front-pluggable cooling units with EMMC onboard and airflow from right to left. The 11850-003 also has a front-removable air filter and features 4x splitters to allow customizing double slots into 2x single slots. Additionally, custom configurations are available upon request.

www.schroff.us

SCHROFF, A BRAND OF PENTAIR ELECTRONIC PACKAGING

8U 19" system enclosure

Model 445 is a member of the VectorPak Series 440 benchtop/rack-mount VME system enclosure series and has a rugged chassis construction. The 8U 19" system enclosure features vertical card insertion for VME, VME64x, and CompactPCI. Model 445 has an uncommitted rear panel for specific rear connector I/O, along with side-recessed handles and lower-rear-access side panels. An optional auxiliary rear exhaust is also possible with the IEEE 1101.10-compliant Model 445.

www.vectorelect.com

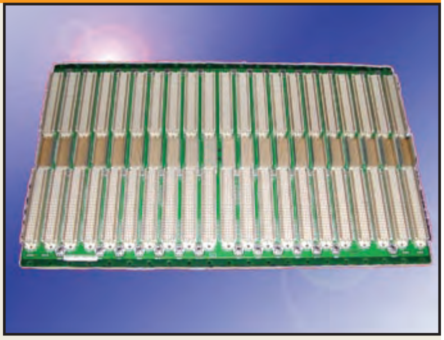
VECTOR ELECTRONICS & TECHNOLOGY, INC.

SFF conduction-cooled chassis

The FS-5973 is a Small Form Factor (SFF) forced-air, conduction-cooled ATR chassis designed for use in avionics environments. Its rugged design features five conduction-cooled 3U slots to IEEE 1101.2, 0.8" pitch; it also has a system slot and four spare slots for I/O and peripherals. Custom mounting options are available for the FS-5973, which meets MIL-STD-5400 Class 1 thermal performance. The chassis can also be customized to meet specifications, including outline and mounting, I/O wiring, I/O panels, custom backplanes, environmental and thermal compliance, and power supplies.

www.aplabs.com **AP LABS**

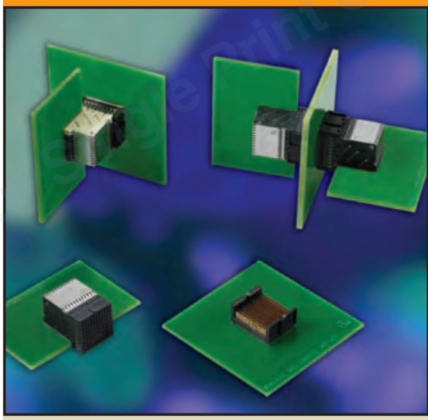
21-slot VME64x backplane



Comtel's VME64x 21 Slot Backplane is designed per ANSI/VITA V 1.1-1997 and includes J1, J2, and J0, along with 10-layer stripline controlled impedance construction. It also features onboard termination without extra width, along with active/passive automatic daisy chain or jumper pin manual daisy chain. The backplane delivers passive 330/470 ohm termination, and high-current power entry taps are positioned near corresponding connector pins for minimum current paths. Rear plug-up long-tail connectors and shrouds are configurable to customer needs, and additional user-defined bus lines per custom requirements are available. The VME64x 21 Slot Backplane also provides an 80 MBps VME64 MBLT data transfer rate and a 160 MBps peak transfer rate using 2edge VME protocol with ETL.

www.comtel-online.de **COMTEL ELECTRONICS GMBH**

Connector system



The ZipLine connector system is designed for both backplane and orthogonal applications. Built upon FCI's AirMax VS technology, ZipLine uses edge-coupling technology to deliver high signal density with low insertion loss and low crosstalk, all without the use of costly and space-consuming metal shields. Data rates can scale from 2.5 Gbps to beyond 12 Gbps without requiring redesign of a basic platform. The connector system includes 84.6 differential signal pairs in a six-pair version on 1.8 mm column pitch, and can go to 101 signal pairs per inch at 1.5 mm column pitch (to be tooled as customers require). The 12 IMLA product offers 72 differential pairs that will fit into a 1" daughtercard pitch. A three-pair, 8 IMLA version is also available and is compatible with a 15 mm card pitch.

www.fciconnect.com **FCI**

MicroTCA backplane connector

MicroTCA-CN080 is a MicroTCA connector utilizing Yamaichi Electronics USA, Inc.'s connector mounting technology, called *Compression Mount Technology* or *CMT*. It requires less backplane inner layers, thus offering outstanding routing capabilities to the MicroTCA system and high-speed transmission of 12.5 Gbps. The connector features metal housing for improved stability, and the backplane's backside can be used for additional components. The connector is designed according to PICMG Spec. MTCA.0 R1.0 and offers insulation resistance of 100 MΩ minutes at 80 Vdc and differential impedance of 100(±) 10Ω. Additionally, it withstands voltages of 80 Vrms a minute. The MicroTCA-CN080 operates at temperature ranges of -55 °C to +105 °C and provides an NE&FE cross-talk ratio of less than 3 percent.

www.yeu.com **YAMAICHI ELECTRONICS USA, INC.**